SIEMENS

SIMATIC

Automation System S7-400 CPU Specifications

Reference Manual

Preface, Contents

Structure of a CPU 41x	1
Special functions of a 41x CPU	2
S7-400 in PROFIBUS DP mode	3
Memory Concept and Startup Scenarios	4
Cycle and Reaction Times of the S7-400	5
Technical Specifications	6
IF 964-DP Interface Submodule	7

Index

This manual is part of the documentation package with the order number **6ES7498-8AA04-8BA0**

Edition 08/2008

Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:



Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.



Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.



Caution

indicates that minor personal injury can result if proper precautions are not taken.

Caution

indicates that property damage can result if proper precautions are not taken.

Notice

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:



Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

Trademarks

SIMATIC®, SIMATIC HMI® and SIMATIC NET® are registered trademarks of SIEMENS AG.

Third parties using for their own purposes any other names in this document which refer to trademarks might infringe upon the rights of the trademark owners.

Copyright Siemens AG 2006 All rights reserved

The reproduction, transmission or use of this document or its contents is not permitted without express written authority. Offenders will be liable for damages. All rights, including rights created by patent grant or registration of a utility model or design, are reserved.

Siemens AGsubsequent editions. Suggestions fIndustry Sectorwelcomed.Postfach 4848Siemens AG 2008D- 90327 NuernbergTechnical data subject to change.

Siemens Aktiengesellschaft

Disclaim of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

A5E00267840

Preface

Purpose of the Manual

The manual contains reference information on operator actions, descriptions of functions and technical specifications of the central processing units, power supply modules and interface modules of the S7-400.

How to configure, assemble and wire these modules (and other) in an S7-400 system is described in the installation manuals for each system.

Required Basic Knowledge

You will need general knowledge of automation to understand this manual.

Target Group

General knowledge in the field of automation technology is presumed.

Prerequisite is also sufficient knowledge in the use of computers or PC-type equipment (programming devices, for example) with Windows 2000 or XP operating system. The S7-400 system is configured in STEP 7 standard software. You should therefore have sufficient knowledge of this standard software. This knowledge is provided in the "Programming with STEP 7" manual.

Please note the information on the safety of electronic control systems in the appendix of this manual, in particular when operating an S7-400 in safety–relevant areas.

Scope of this Manual

The manual applies to the S7-400 automation system, including the following CPUs:

- CPU 412-1; (6ES7412-1XF04-0AB0)
- CPU 412-2; (6ES7412-2XG04-0AB0)
- CPU 414-2; (6ES7414-2XG04-0AB0)
- CPU 414-3; (6ES7414-3XJ04-0AB0)
- CPU 416-2; (6ES7416-2XK04-0AB0)
- CPU 416-2F; (6ES7416-2FK04-0AB0)
- CPU 416-3; (6ES7416-3XL04-0AB0)
- CPU 417-4; (6ES7417-4XL04-0AB0)

Approvals

You can find details on approvals and standards in the "Module Data" reference manual.

Place of this Documentation in the Information Environment

This manual is part of the documentation package for S7-400.

System	Documentation Package	
S7-400	S7-400 Programmable Controller; Hardware and Installation	
	• S7-400 Programmable Controllers; Module Data	
	Automation System S7-400; CPU Data	
	S7-400 Instruction List	

Navigating

The manual offers the following access help to make it easy for you to find specific information:

- At the start of the manual you will find a complete table of contents and a list of the diagrams and tables that appear in the manual.
- An overview of the contents of each section is provided in the left column on each page of each chapter.
- You will find a glossary in the appendix at the end of the manual. The glossary contains definitions of the main technical terms used in the manual.
- At the end of the manual you will find a comprehensive index which gives you rapid access to the information you need.

	I
Standard Software	Installing and commissioning STEP 7 on a programming device / PC
for S7	Working with STEP 7 in the following context:
STEP 7 Basics	Project and file management
	S7-400 configuration and parameter assignment
	Assigning symbolic names to user programs
	Creating and testing a user program in STL/LAD
	Creating data blocks
	Configuring the communication between CPUs
	Downloading, uploading, saving and deleting user programs on the CPU / programming device
	Monitoring and controlling user programs
	Monitoring and controlling the CPU
	 Guide to the efficient implementiation of programming tasks using the programming device / PC and STEP 7
	• Operating principle of the CPUs (for example, memory concept, I/O access, addressing, blocks, data management)
	Description of STEP 7 data management
	Using data types of STEP 7
	Using linear and structured programming
	Using block call instructions
	• Utilizing debug and diagnostic functions of the CPUs in the user program (for example, error OBs, status word)
STEP 7 Reference Information	• Basics on working with STL, LAD, or FBD (for example, structure of STL, LAD, or FBD, number formats, syntax)
Statement List (STL)	Description of all STEP 7 instructions (with program examples)
for S7-300 and	Description of the various addressing options of STEP 7 (with examples)
S7-400	Description of the internal registers in the CPU
Ladder Logic (LAD) for S7-300 and	Description of all integrated system / standard functions of the CPUs
S7-400	Description of all integrated organization blocks of the CPUs
Function Block Diagram (FBD) for S7-300 and S7-400	
System and Standard Functions	

Recycling and Disposal

The S7-400 is low in contaminants and can therefore be recycled. To recycle and dispose of your old device in an environment-friendly manner, please contact a disposal company certified for disposal of electronic waste.

Further Support

If you have any further questions related to the use of your product for which you have not found an answer in this documentation, please contact your Siemens partner at your local Siemens office.

You can find your contact partner under:

http://www.siemens.com/automation/partner

A guide to out technical documentation for the various SIMATIC products and systems is found under:

http://www.siemens.de/simatic-tech-doku-portal

The online catalog and order system is found under:

http://mall.ad.siemens.com

Training Centers

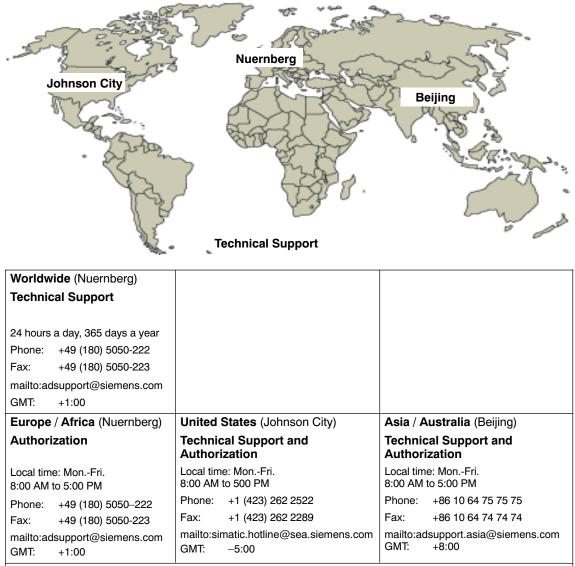
We offer various courses to newcomers to the SIMATIC S7 programmable logic controller. For details, please contact your regional training center or our central training center in D 90327 Nuremberg, Germany:

Phone: +49 (911) 895-3200.

Internet: http://www.sitrain.com

A&D Technical Support

Worldwide, available 24 hours a day:



The languages of the SIMATIC Hotlines and the authorization hotline are generally German and English.

Service & Support on the Internet

In addition to our documentation, we offer our Know-how online on the internet at:

http://www.siemens.com/automation/service&support

where you will find the following:

- The newsletter, which constantly provides you with up-to-date information on your products.
- The right documents via our Search function in Service & Support.
- A forum, where users and experts from all over the world exchange their experiences.
- Your local representative for Automation & Drives.
- Information on field service, repairs, spare parts and more under "Services".

Contents

1	Structu	re of a CPU 41x	1-1
	1.1	Control and display elements of the CPUs	1-2
	1.2	Monitoring functions of the CPU	1-8
	1.3	Status and error displays	1-10
	1.4	Mode selector switch	1-13
	1.5	Structure and function of the Memory Card	1-17
	1.6	Multipoint Interface (MPI)	1-21
	1.7	PROFIBUS DP Interface	1-22
	1.8	Overview of the Parameters for the S7-400 CPUs	1-23
2	Special	functions of a 41x CPU	2-1
	2.1	Reading Service Data	2-2
	2.2 2.2.1 2.2.2 2.2.3	Multicomputing Peculiarities Peculiarities Multicomputing Multicomputing Interrupt Configuring and programming multicomputing Operation Multicomputing	2-3 2-5 2-6 2-6
	2.3	Modifications to the System During Operation	2-7
3	S7-400 i	in PROFIBUS DP mode	3-1
	3.1 3.1.1 3.1.2 3.1.3 3.1.4 3.1.5 3.1.6	CPU 41x as DP Master/DP Slave DP address areas of 41x CPUs 41x CPU as PROFIBUS DP master Diagnostics of the CPU 41x as DP Master CPU 41x as DP Slave Diagnostics of the CPU 41x as DP Slave CPU 41x as DP slave: Station States 1 to 3	3-2 3-3 3-4 3-8 3-13 3-18 3-24
	3.2 3.2.1 3.2.2	Direct Communication Principle of Direct Data Diagnostics in Direct Communication	3-31 3-31 3-32
	3.3 3.3.1 3.3.2 3.3.3 3.3.4	Consistent Data Consistency for Communication Blocks and Functions Access to the Working Memory of the CPU Reading from and Writing to a DP Standard Slave Consistently Writing Data Consistently to a DP Standard Slave Using SFC 15 "DPWR_DAT"	3-34 3-35 3-35 3-35 3-36
	3.3.5	Consistent Data Access without the Use of SFC 14 or SFC 15	3-37

4	Memory	Concept and Startup Scenarios	4-1
	4.1	Overview of the Memory Concept of S7-400 CPUs	4-2
	4.2	Overview of the Startup Scenarios for S7-400 CPUs	4-5
5	Cycle ar	nd Reaction Times of the S7-400	5-1
	5.1	Cycle Time	5-2
	5.2	Cycle Time Calculation	5-4
	5.3	Different Cycle Times	5-7
	5.4	Communication Load	5-9
	5.5	Reaction Time	5-12
	5.6	How Cycle and Reaction Times Are Calculated	5-17
	5.7	Examples of Calculating the Cycle Time and Reaction Time	5-18
	5.8	Interrupt Reaction Time	5-21
	5.9	Example of Calculating the Interrupt Reaction Time	5-23
	5.10	Reproducibility of Time-Delay and Watchdog Interrupts	5-24
6	Technic	al Specifications	6-1
	6.1	Technical Specifications of the CPU 412-1; (6ES7412-1XF04-0AB0)	6-2
	6.2	Technical Specifications of the CPU 412-2; (6ES7412-2XG04-0AB0)	6-6
	6.3	Technical Specifications of the CPU 414-2; (6ES7414-2XG04-0AB0)	6-10
	6.4	Technical Specifications of the CPU 414-3; (6ES7414-3XJ04-0AB0)	6-14
	6.5	Technical Specifications of the CPU 416-2; (6ES7416-2XK04-0AB0, 6ES7416-2FK04-0AB0)	6-18
	6.6	Technical Specifications of the CPU 416-3; (6ES7416-3XL04-0AB0)	6-22
	6.7	Technical Specifications of the CPU 417-4; (6ES7417-4XL04-0AB0)	6-26
	6.8	Technical Specifications of the Memory Cards	6-31
7	IF 964-D	P Interface Submodule	7-1
	7.1 7.1.1 7.1.2	IF 964-DP Interface Submodule for S7-400 Pin Assignments Technical Specifications	7-2 7-3 7-4
			dex-1

Figures

1-1	Layout of the control and display elements of a 412-1 CPU	1-2
1-2	Layout of the control and display elements of the 41x-2 CPU	1-3
1-3	Layout of the control and display elements of the 41x-3 CPU	1-4
1-4	Layout of the control and display elements of the 417-4 CPU	1-5
1-5	Positions of the mode selector switch	1-13
1-6	Structure of the Memory Card	1-17
2-1	Multicomputing Example	2-4
2-2	Overview: Architecture enabling modification	
	of a system during operation	2-7
3-1	Diagnostics with CPU 41x	3-10
3-2	Diagnostic Addresses for the DP Master and DP Slave	3-11
3-3	Intermediate Memory in the CPU 41x as DP Slave	3-14
3-4	Diagnostic Addresses for the DP Master and DP Slave	3-21
3-5	Structure of the Slave Diagnosis	3-23
3-6	Structure of the Module Diagnosis of the CPU 41x	3-27
3-7	Structure of the Station Diagnosis	3-28
3-8	Bytes +4 to +7 for Diagnostic and Process Interrupts	3-29
3-9	Direct Communication with CPUs 41x	3-31
3-10	Diagnostic Address for the Recipient During Direct Communication	3-32
5-1	Parts and Composition of the Cycle Time	5-3
5-2	Different Cycle Times	5-7
5-3	Minimum Cycle Time	5-8
5-4	Formula: Influence of Communication Load	5-9
5-5	Breakdown of a Time Slice	5-9
5-6	Dependency of the Cycle Time on the Communication Load	5-11
5-7	DP Cycle Times on the PROFIBUS-DP Network	5-13
5-8	Shortest Reaction Time	5-14
5-9	Longest Reaction Time	5-15
5-10	Calculating the Interrupt Reaction Time	5-21
7-1	IF 964-DP Interface Submodule	7-2

Tables

1-1	LEDs of the CPUs	1-6
1-2	Positions of the mode selector switch	1-13
1-3	Security classes of an S7-400 CPU	1-14
1-4	Types of Memory Cards	1-18
3-1	CPUs 41x (MPI/DP Interface as PROFIBUS DP)	3-3
3-2	CPUs 41x (MPI/DP Interface and DP Module as PROFIBUS DP)	3-3
3-3	Meaning of the BUSF LED of the CPU 41x as DP Master	3-8
3-4	Reading Out the Diagnosis with STEP 7	3-9
3-5	Event Detection of the CPUs 41x as DP Master	3-12
3-6	Configuration Example for the Address Areas	
	of the Intermediate Memory	3-15
3-7	Meaning of the BUSF LEDs of the CPU 41x as DP Slave	3-18
3-8	Reading Out the Diagnostic Data with STEP 5 and STEP 7	
	in the Master System	3-19
3-9	Event Detection of the CPUs 41x as DP Slave	3-22
3-10	Evaluation of RUN-STOP Transitions in the DP Master/DP Slave	3-22
3-11	Structure of the Station Status 1 (Byte 0)	3-24
3-12	Structure of Station Status 2 (Byte 1)	3-25
3-13	Structure of Station Status 3 (Byte 2)	3-25
3-14	Structure of the Master PROFIBUS Address (Byte 3)	3-25
3-15	Structure of the Manufacturer ID (Bytes 4, 5)	3-26
3-16	Event Detection of the CPUs 41x as	
	Recipient During Direct Communication	3-32
3-17	Evaluation of the Station Failure in the	
	Sender During Direct Communication	3-33
4-1	Memory Requirements	4-3
5-1	Cyclic Program Scanning	5-3
5-2	Factors that Influence the Cycle Time	5-4
5-3	Portions of the process image transfer time	5-5
5-4	Operating system scan time at scan cycle checkpoint	5-6
5-5	Increase in Cycle Time by Nesting Interrupts	5-6
5-6	Reducing the Reaction Time	5-16
5-7	Example of Calculating the Reaction Time	5-18
5-8	Hardware Interrupt and Diagnostic Interrupt Reaction Times;	
	Maximum Interrupt Reaction Time Without Communication	5-21
5-9	Reproducibility of Time-Delay and Watchdog Interrupts of the CPUs.	5-24
7-1	X1 Socket, IF 964-DP (9-Pin Sub D Connector)	7-3

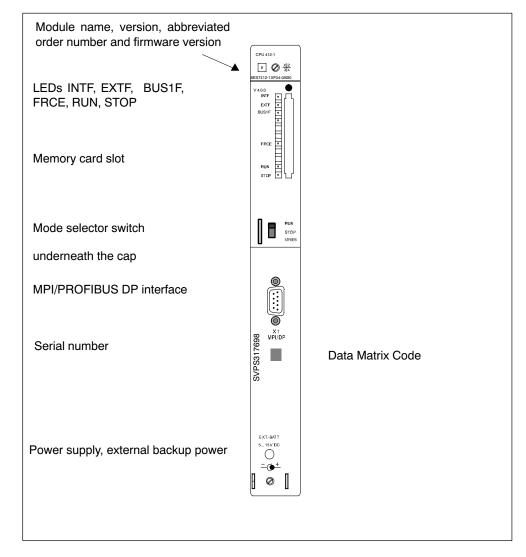
1

Structure of a CPU 41x

Chapter Overview

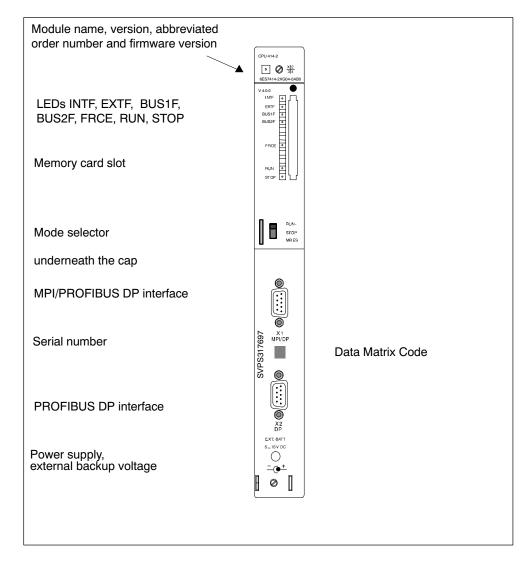
In Section	You Will Find	On Page
1.1	Control and display elements of the CPUs	1-2
1.2	Monitoring functions of the CPU	1-8
1.3	Status and error displays	1-10
1.4	Mode selector switch	1-13
1.5	Structure and function of the Memory Card	1-17
1.6	Multipoint Interface (MPI)	1-21
1.7	PROFIBUS DP Interface	1-22
1.8	Overview of the Parameters for the S7-400 CPUs	1-23

1.1 Control and display elements of the CPUs



Controls and display elements of the 412-1 CPU

Figure 1-1 Layout of the control and display elements of a 412-1 CPU



Controls and display elements of the 41x-2 CPU

Figure 1-2 Layout of the control and display elements of the 41x-2 CPU



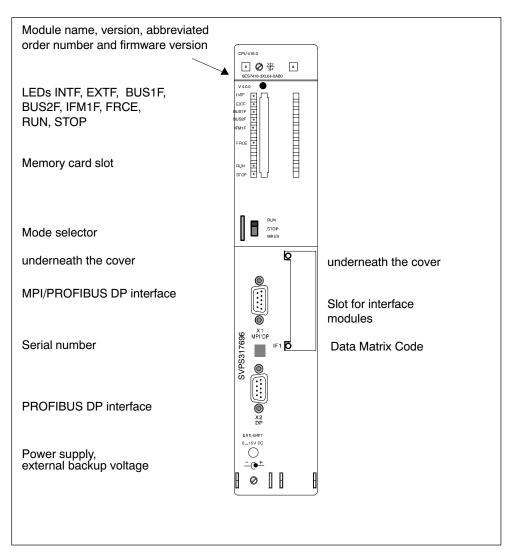
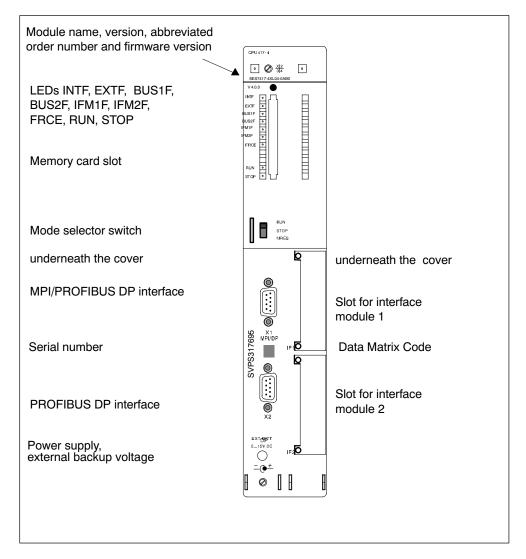


Figure 1-3 Layout of the control and display elements of the 41x-3 CPU



Controls and display elements of the 417-4 CPU

Figure 1-4 Layout of the control and display elements of the 417-4 CPU

LED displays

Table 1-1 gives you an overview of the LEDs on the individual CPUs.

Section 1.2 describes the states and errors indicated by these LEDs.

LED Cold		Color Meaning		CPU			
			412-1	412-2 414-2 416-2	414-3 416-3	417-4	
INTF	red	Internal error	x	х	х	х	
EXTF	red	External error	x	х	х	x	
FRCE	yellow	Active force request	x	х	х	х	
RUN	green	RUN mode	x	х	х	х	
STOP	yellow	STOP mode	x	х	х	х	
BUS1F	red	Bus error at MPI/PROFIBUS DP interface 1	x	x	х	x	
BUS2F	red	Bus error at PROFIBUS DP interface 2	-	x	х	x	
IFM1F	red	Error at interface submodule 1	_	_	х	x	
IFM2F	red	Error at interface submodule 2	_	-	-	х	

Table 1-1LEDs of the CPUs

Mode selector switch

You can use the mode selector to select the current operating mode of the CPU. The mode selector is a three-position toggle switch.

Section 1.4 describes the functions of the mode selector switch.

Memory Card slot

You can insert a memory card into this slot.

There are two types of Memory Card:

RAM cards

For the expansion of CPU load memory.

FLASH cards

Non-volatile memory for storing the user program and data (retentive without backup battery). You can either program the FLASH card on the programming device or in the CPU. The FLASH card also expands the load memory of the CPU.

For a detailed description of the Memory Cards, refer to Chapter 1.5.

Slot for Interface Modules

This slot holds one interface module (IF module) for 1x-3 and 41x-4 CPUs .

MPI/DP interface

Devices you can connect to the MPI interface of the CPU, for example:

- Programming devices
- Control and monitoring devices
- Further S7-400 or S7-300 PLCs (see chapter 1.6).

Use the bus connector with angular cable outlet (see the manual *Hardware and Installation*, Chapter 7)

You can also configure the MPI interface as DP master in order to use it as PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP interface

Lets you connect the distributed I/O, programming devices/OPs and further DP master stations.

POwer supply, external backup voltage at the "EXT.-BATT." connector

You can install either one or two backup batteries in the S7-400 power supply modules, depending on the module type. By doing so, you:

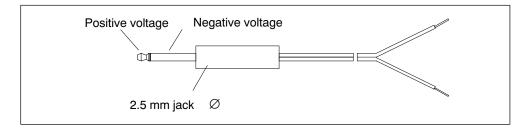
- Backup the user program in RAM memory.
- Retain the values of flags, timers, counters, system data and data of dynamic DBs.
- Backup the internal clock.

You can achieve the same effects by supplying a voltage between 5 V DC and 15 V DC to the "EXT.-BATT." connector of the CPU.

Properties of the "EXT.-BATT." input:

- Polarity reversal protection
- Short-circuit current limited to 20 mA

You need a cable with a 2.5 mm \emptyset jack to connect the power suplpy to the "EXT.-BATT" socket, as shown in the following illustration. Note the polarity of the jack.



Note

You require the external power supply to the "EXT.-BATT." socket when you replace a power supply module and want to backup the user program in RAM and the data mentioned earlier while you are replacing the module.

1.2 Monitoring functions of the CPU

Monitoring and error messages

The CPU hardware and the operating system monitoring functions ensure proper functioning of the system and a defined reaction to errors. Certain error events will also trigger a reaction in the user program. When recursive errors occur, the LED is switched off with the next incoming error.

The table below provides an overview of possible errors, their causes and the reactions of the CPU.

Type of Fault/Error	Cause of Fault	Response of the Operating System	Error LED
Access error , incoming	Module failure (SM, FM, CP) I/O write access error I/O read access error	 The "EXTF" LED stays lit until the error is acknowledged. In SMs: Call of OB122 Entry in the diagnostic buffer At input modules: "NULL" entry of for the date in the accumulator or the process image On other modules: Call of OB122 	EXTF
Time-out error, incoming	 The user program execution time (OB1 and all interrupt and error OBs) exceeds the specified maximum cycle time. OB request error Overflow of the startup buffer Watchdog interrupt Resume RUN after CiR 	The "INTF" LED is lit until the error is acknowledged. Call of OB80 If this OB is not loaded: The CPU goes into STOP.	INTF
Faulty power supply module(s) (not mains failure), incoming and outgoing error	 In the central or distributed I/O rack: At least one backup battery of the power supply module is low. Backup voltage is missing. The 24 V DC supply of the power supply module has failed. 	Call of OB81 If this OB is not loaded: The CPU continues RUN.	EXTF
Diagnostic Interrupt (incoming and outgoing)	An I/O module with interrupt capability reports a diagnostic interrupt.	Call of OB82 If this OB is not loaded: The CPU goes into STOP.	EXTF
Removal /insertion interrupt (incoming and outgoing)	Removal or insertion of an SM and insertion of the wrong module type. The LED EXTF will not light up if only one SM is installed and then removed while the CPU is in STOP (default configuration). The LED lights up briefly when the SM is inserted again.	Call of OB83 If the OB is not loaded: The CPU goes into STOP mode.	EXTF
CPU Hardware error (incoming)	 A memory error was detected and eliminated 	Call of OB84 If this OB is not loaded: The CPU continues RUN.	INTF
Priority class error (Only incoming, depending on the OB85 mode	 A priority class is called, but the corresponding OB is not available. In the case of an SFB call: The instance DB is missing or faulty. 	Call of OB85 If this OB is not loaded: The CPU goes into STOP.	INTF

Type of Fault/Error			Error LED
or incoming and outgoing)	Error while updating the process image		EXTF
Rack / station failure (incoming and outgoing)	 Power failure on an expansion module DP segment error Failure of a coupling segment: missing or defective IM, cable break) 	Call of OB86 If this OB is not loaded: The CPU goes into STOP.	EXTF
Communication error (incoming)	 Unable to enter status information in the DB Invalid message frame ID Frame length error Error in the structure of the shared datagram DB access error 	Call of OB87	INTF
Execution cancelled (incoming)	 Synchronous error nesting depth exceeded Too many nested block calls (B stack) Error when allocating local data 	Call of OB88 If the OB is not loaded: The CPU goes into STOP mode.	INTF
Programming error (incoming)	 Error in the machine code or user program: BCD conversion error Range length error Range error Alignment error Write error Timer number error Counter number error Block number error Block not loaded 	Call of OB121 If the OB is not loaded: The CPU goes into STOP mode.	INTF
Code error (incoming)	Error in the compiled user program (e.g. ilegal OP code or a jump has violated block boundaries)	CPU goes into STOP mode. Restart or CPU memory reset required.	INTF
Loss of the clock signal (incoming)	When using clock sync mode: The clock signal was lost either because OB61 64 was not started due to higher priorities, or because additional asynchronous bus loads suppressed the bus clock.	Call of OB80 If the OB is not loaded: The CPU goes into STOP Call of OB 6164 at the next pulse.	INTF EXTF

Further test and information functions are available in each CPU and can be called in STEP 7.

1.3 Status and error displays

Status displays

The two RUN and STOP LEDs on the front panel of the CPU indicate the current CPU operating state.

LED		Meaning	
RUN	STOP		
Н	D	CPU is in RUN.	
D	Н	CPU is in STOP. The user program is not processed. Restart and warm restart/reboot is possible. If the STOP status was triggered by an error, the error indication (INTF or EXTF) is also set.	
В	В	CPU status is FAULTY. The INTF, EXTF and FRCE LEDs also flash.	
2 Hz	2 Hz		
В	н	CPU HOLD was triggered by a test function.	
0.5 Hz			
В	Н	A warm restart / cold restart / hot restart was triggered. It can take a	
2 Hz		minute or longer to execute these functions, based on the length of the OB called. If the CPU still does not go into RUN, there might be an error in the system configuration.	
x	В	The CPU requests memory reset.	
	0.5 Hz		
x	В	CPU memory reset is active.	
	2 Hz		

D = LED is dark; H = LED is lit; B = LED flashes at the specified frequency; x = LED status is irrelevant

Error displays and special features, all CPUs

The three LEDs INTF, EXTF and FRCE on the front panel of the CPU indicate errors and special features in user program execution.

LED			Meaning
INTF	EXTF	FRCE	
Н	x	x	An internal error was detected (program or configuration error) or the CPU is performing a CiR.
x	Н	x	An external error was detected (that is, the cause of error cannot be traced back to the CPU module).
x	х	Н	A force job is active.

H = LED is lit; x = LED status is irrelevant

The LEDs BUSF1 and BUSF2 indicate errors at the MPI/DP and PROFIBUS DP interfaces.

LED		Meaning		
BUS1F	BUS2F			
Н	x	An error was detected at the MPI/DP interface.		
x	Н	An error was detected at the PROFIBUS DP interface.		
В	x	DP master: One or more slaves at PROFIBUS DP interface 1 are not responding. DP slave: not addressed by the DP master		
×	В	DP master: One or more slaves at PROFIBUS DP interface 2 are not responding. DP slave: not addressed by the DP master		

H = LED is lit; B = LED flashes; x = LED status is irrelevant

Error displays and special features, 41x-3 and 41x-4 CPUs

41x-3 and 41x-4 CPUs are still equipped with the IFM1F or IFM1F and IFM2F LEDs. These indicate errors at the first and second IFM.

LED		Meaning	
IFM1F	IFM2F		
Н	x	An error was detected at module interface 1.	
x	Н	An error was detected at module interface 2.	
В	x	DP master: DP slave:	No response from one or several slaves connected to the PROFIBUS DP interface module in slot 1 not addressed by the DP master
x	В	DP master: DP slave:	No response from one or several slaves conected to the PROFIBUS DP interface in slot 2 not addressed by the DP master

H = LED is lit; B = LED flashes; x = LED status is irrelevant

Diagnostic buffer

In STEP 7, you can select "PLC -> Module status" to read the cause of an error from the diagnostic buffer.

1.4 Mode selector switch

Function of the mode selector switch

The mode selector switch can be used to set the CPU to RUN or STOP mode, or to reset the CPU memory. STEP 7 offers further mode selection options.

Positions

The mode selector switch is a toggle switch. Figure 1-5 shows the positions of the mode selector switch.

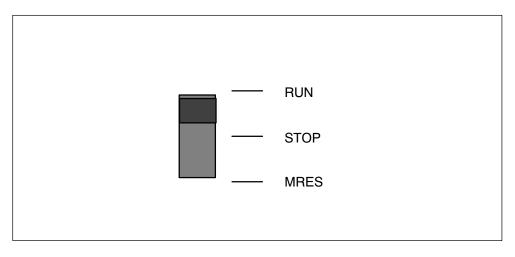


Figure 1-5 Positions of the mode selector switch

Table 1-2 describes the positions of the mode selector switch. In the event of a fault or if there are problems preventing a startup, the CPU goes into STOP or retain this mode, regardless of the position of the mode selector switch.

Table 1-2 Positions of the mode selector switch

Position	Explanation
RUN	If there is no startup problem or error and the CPU was able to go into RUN, the CPU either executes the user program or remains idle.
	 You can upload programs from the CPU to the programming (CPU -> PG) You can upload programs from the PG to the CPU (PG -> CPU).
STOP	 The CPU does not execute the user program. The digital signal modules are locked. Programs can: You can upload programs from the CPU to the programming (CPU -> PG) You can upload programs from the PG to the CPU (PG -> CPU).
MRES (CPU memory reset; Master Reset)	Momentary-contact position of the toggle switch for CPU memory reset (see below).

Security classes

A security class can be agreed for S7-400 CPUs in order to prevent unauthorized access to CPU programs. You can define a security class which allows users access to PG functions without particular authorization (password). On password level you can access all PG functions.

Setting the security classes

You can set the security classes (1 to 3) for a CPU by calling STEP 7 \rightarrow HW Config.

You can delete the the security class set STEP 7 -> HW Config by means of a manual reset using the mode selector switch.

Table 1-3 lists the security classes of an S7-400 CPU.

Table 1-3 Security classes of an S7-400 CPU

Security class	Function
1	Access to all programming device functions is allowed (default).
2	 Objects may be uploaded from the CPU to the PG. That is, only the read–only functions can be accessed on the PG.
	 Access to process control, process monitoring and process communication functions is allowed.
	Access to the information functions is allowed.
3	 Access to process control, process monitoring and process communication functions is allowed.
	Access to the information functions is allowed.

Sequence for CPU memory reset

Case A: You want to download all data of a new user program to the CPU.

1. Set the switch to STOP.

Result: The STOP LED is lit.

2. Set the switch to MRES setting and hold it at this position.

Result: The STOP LED performs this cycle: 1 sec OFF -> 1 sec ON -> 1 sec OFF -> continuous signal.

3. Reset the switch to STOP, then set MRES again within the next 3 seconds, then reset it to STOP.

Result: The STOP LED flashes at least 3 seconds at 2 Hz (memory reset is being executed), then its signal is set continuously.

Case B: The CPU requests memory reset, indicated by the flashing STOP LED (5 Hz). The system requests a CPU memory reset after a memory card was removed or inserted, for example.

Set the switch to MRES and then return it to STOP.

Result: The STOP LED flashes at least 3 seconds at 2 Hz (memory reset is being executed), then its signal is set continuously.

For detailed information on CPU memory reset refer to chapter 6 of the manual *S7-400 Programmable Controllers Hardware and Installation*.

CPU sequence for memory reset

The CPU performs the following processes for memory reset:

- It deletes the user program from work memory and in load memory (integrated RAM or RAM Card).
- It deletes all counters, flags and timers (except the time).
- It performs a hardware selftest.
- It initializes the hardware and system program parameters, that is, its internal default settings. Some of the configured defaults are taken into account.
- When a FLASH Card is inserted and after the CPU memory reset is completed, the CPU loads the user program and the system parameters from the FLASH Card to work memory.

What is retained after a CPU memory reset...

The following data are retained:

- The contents of the diagnostics buffer can be read by uploading it to the PG in STEP 7.
- The parameters of the MPI interface (MPI address and highest MPI address). Note the special features shown in the table below.
- The time
- The status and value of the operating hours counter

Special feature: MPI parameters

A special situation is given for the MPI parameters when a CPU memory reset is preformed. The table below shows which MPI parameter remain valid after a CPU memory reset.

CPU memory reset	MPI parameters	
with FLASH Card	, stored on the FLASH Card are valid	
without FLASH Card	are retained in the CPU and valid	

Cold start

- During a cold start, all data (process image, flags, timers, counters and DBs) are reset to the start values stored in the program in load memory, regardless whether these are configured as retentive or non-retentive data.
- Program execution is restarted at the start position (OB100, OB101, OB102 or OB1).

Restart (warm start)

• A restart resets the process image and the non-retentive flags, timers, times and counters.

Retentive flags, times and counters retain their last valid value.

All DBs assigned the "Non Retain" attribute are reset to load values. The remaining DBs retain their last valid value.

- Program execution is restarted at the start position (startup OB or OB 1).
- After a power supply interruption, the warm restart function is only available in backup mode.

Hot restart

- When a hot restart is performed, all data and the process image retain their last valid value.
- Program execution is resumed at the breakpoint.
- The outputs do not change their status until the current cycle is completed.
- After a power supply interruption, the hot restart function is only available in backup mode.

Control sequence for restart (warm restart)

1. Set the switch to STOP.

Result: The STOP LED is lit.

2. Set the switch to RUN.

Control sequence for hot restart

1. Select "hot restart" via PG.

The correspondend button can be used only if a hot restart is possible whith your CPU.

Control sequence for cold restart

A cold start can only be initiated on the PG.

1.5 Structure and function of the Memory Card

Order numbers

The order numbers for memory cards are listed in chapter 6 of the technical specification.

Configuration

The memory card is slightly larger than a credit card and protected by a strong metal casing. It is inserted into a front slot of the CPU. The memory card casing is encoded to allow only one position of insertion.

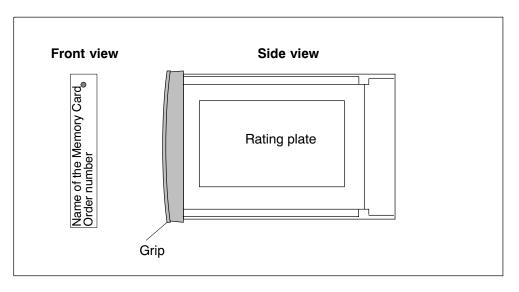


Figure 1-6 Structure of the Memory Card

Function

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. In operation, the load memory contains the entire user program, including comments, symbols, special additional information that permits decompilation of the user program, and all the module parameters (see chapter 4.1).

What is stored on the Memory Card?

The following data can be stored on the memory card:

- User program, that is, blocks (OBs, FBs, FCs, DBs) and system data
- · Parameters which determine the behavior of the CPU
- Parameters which determine the behavior of the I/O modules.
- In STEP 7 V5.1 or higher, all project data on suitable Memory Cards.

Types of Memory Cards for S7-400

Two types of memory card are used in the S7-400:

- RAM cards
- Flash cards (FEPROM cards)

Note

Non-Siemens memory cards cannot be used in the S7-400.

What type of Memory Card should I use?

Whether you use a RAM card or a Flash card depends on your application.

Table 1-4	Types of I	Memory Cards
-----------	------------	--------------

If you	Then
want to store the data in RAM and edit your program in RUN,	use a RAM card
want to backup your user program permanently on the memory card (without backup battery or outside the CPU),	use a Flash card

RAM Card

To use a RAM card and load the user program, you must insert it into the CPU slot. The user program is loaded with the help of the programming device (PG).

You can load the entire user program or individual elements such as FBs, FCs, OBs, DBs, or SDBs to the load memory in when the CPU is in STOP mode or RUN.

All data on the RAM Card are lost when you remove it from the CPU. The RAM card does not have a built-in backup battery.

If the power supply has a functioning backup battery or an external backup voltage is supplied to the CPU via the "EXT. BATT." socket, the contents of the RAM card are retained after power is switched off, provided the RAM card stays in the CPU and the CPU stays in the rack.

Flash Card

With a Flash card, you have two options of loading the user program:

- Set the CPU to STOP using the mode selector, plug the Flash card into the CPU, then load the user program with STEP 7 "PLC -> Load User Program to Memory Card".
- Load the user program into the Flash card in offline mode at the programming device or adapter and then insert the Flash card into the CPU.

You can only reload the full user program using the Flash card. You can load smaller program sections into the integrated load memory on the CPU using the programming device. In the case of extensive program changes, you must always reload the Flash card with the full user program.

The Flash card does not require a backup voltage, that is, the information stored on it is retained even when you remove the Flash card from the CPU or if you operate your S7-400 system without a buffering function (without backup battery in the power supply module or "EXT. BATT." socket of the CPU).

Which Memory Card Capacity to Use

The capacity of the memory card is determined by the size of the user program and the additional memory requirements when using function modules or communications modules. For information on memory requirements, refer to the relevant module manuals.

To optimze utilization of work memory (code and data) on your CPU, you should expand the load memory of the CPU with a memory card which has at least the same capacity as the work memory.

Changing the Memory Card

To change the memory card:

- 1. Set the CPU to STOP.
- 2. Remove the memory card.

Note

If you remove the memory card, the CPU requests a memory reset in a 3-sec sequence, which is indicated by the flashing STOP LED. This sequence cannot be influenced by error OBs.

- 3. Insert the "new" memory card.
- 4. Reset CPU memory.

1.6 Multipoint Interface (MPI)

Connectable devices

You can connect the following stations to the MPI, for example:

- Programming devices (PG/PC)
- Control and monitoring devices (OPs and TDs)
- Additional SIMATIC S7 PLCs

Some devices use the 24 V DC power supply of the interface. This voltage connected to a reference potential.

PG/OP->CPU communication

A CPU is capable of maintaining several simultaneous online connections. Only one of these connections is reserved as default connection for a PG, and a second for the OP/ control and monitoring device.

For CPU-specific information on the number of connection resources of connectable OPs, refer to chapter 6 of the Technical Specifications.

Communication and interrupt response times

Notice

The interrupt reaction times may be extended by read / write operations involving the maximum data length (approx. 460 byte).

CPU -> CPU communication

There are three types of CPU-CPU communication:

- Data transfer by means of S7 basic communication
- Data transfer by means of S7 communication
- Data transfer by means of global data communication

For further information, refer to the "Programming with STEP 7" manual.

Connectors

Always use bus connectors with angular cable outlet PROFIBUS DP or PG cables used to connect devices to the MPI (see chapter 7 of the manual *Hardware and Installation*).

Multipoint interface as DP interface

You can also configure the MPI interface for operation as DP interface. To do so, you can reconfigure the MPI interface in SIMATIC Manager of STEP 7. You can use this to set up a DP segment consisting of up to 32 slaves.

1.7 **PROFIBUS DP Interface**

Connectable devices

You can connect any compliant DP slave to the PROFIBUS DP interface.

Here, the CPU is operated either as a DP master or a DP slave which is connected via PROFIBUS DP field bus to the passive slave stations or other DP masters.

Some devices use the 24 V DC power supply of the interface. This voltage connected to a reference potential.

Connectors

Always use the bus connector for PROFIBUS DP or PROFIBUS cables used to connecting devices to the PROFIBUS DP interface (see chapter 7 of the manual *Hardware and Installation*).

1.8 Overview of the Parameters for the S7-400 CPUs

Default values

All parameters are assigned factory settings. These defaults are suitable for a whole range of standard applications, that is, an S7-400 can be used immediately as turnkey system which does not require any further settings.

You can define CPU-specific default values using the "HW Config" tool in STEP 7.

Parameter Blocks

The behavior and properties of the CPU are declared in the parameters which are stored in system data blocks. The CPUs are assigned default values. You can edit these default values by changing the parameters in HW Config.

The list below provides an overview of the configurable system properties of the CPUs.

- General properties (for example, the CPU name)
- Startup (for example, enabling a hot restart)
- Constant bus cycle time interrupts
- Cycles / memory flags (e.g. scan cycle cycle monitoring time)
- Retentivity (number of retentive tags, timers and counters)
- Memory (e.g. local data)

Note: If you change the work memory allocation by modifying parameters, this work memory is reorganized when you load system data to the CPU. The result is, that the DBs which were generated by an SFC will be deleted, and the remaining DBs are assigned default initial values from load memory.

Work memory space available for storing code or DBs can be reorganized when system data are loaded by changing the following parameters:

- Size of the process image (byte-oriented; on the "Cycle / clock flag" tab)
- Communication resources (on the "Memory" tab)
- Size of the diagnostics buffers (on the "Diagnostics / clock" tab)
- The amount of local data for all priority classes ("Memory" tab)
- Assignment of interrupts (process interrupts, delay interrupts, asynchronous error interrupts) to the priority classes
- Time-of-day interrupts (e.g. start, interval duration, priority)
- Watchdog interrupts (e.g. priority, interval duration)
- Diagnostics/clock (e.g. time synchronization)
- Protection levels

Note

16 memory bytes and 8 counter numbers are set to retentive in the default settings, in other words, they are not deleted when the CPU is restarted.

Parameter Assignment Tool

You can set the individual CPU parameters using "Configuring Hardware" in STEP 7.

Note

If you make changes to the existing settings of the following parameters, the operating system carries out initializations like those during cold restart.

- Size of the process image of the outputs
- Size of the process image of the inputs
- Size of the local data
- Number of diagnostic buffer inputs
- Communication resources

These initializations are:

- Data blocks are initialized with the load values
- Memory bits, times, counts, inputs and outputs are deleted regardless of the retentive settings (0)
- DBs generated via SFC are deleted
- Permanently configured, base communication connections are established
- All the priority classes start from the beginning again

2

Special functions of a 41x CPU

Chapter Overview

In Section	You Will Find	On Page
2.1	Read Service Data	2-2
2.2	Multicomputing	2-3
2.3	Modifications to the System During Operation	2-7

2.1 Reading Service Data

Requirements

This function requires STEP 7 V5.3 or higher.

When is this function used?

If you require service support, please contact your Siemens Customer Support Center. The Customer Support Center may request specific information about the status of the CPU in your system for analysis. This information is stored in the diagnostics buffer and in the actual service data.

Select the "PLC -> Save service data" menu command to read this information, then save the data to two files and send these to your Customer Support Center.

Please note:

- You should save all service data immediately after the CPU has changed to STOP, or when a redundant system has lost its synchronization.
- Always save the service data of both CPUs in the redundant system, that is, including the data of the CPU which is still in RUN after synchronization is lost.

The service data are written to the file <filename.ext> in the <pathname> path.

Procedure

1. Select the "PLC -> Save service data" menu command

A dialog box opens where you can define a storage location and name for both files.

- 2. Save the files.
- 3. Send these files to your Customer Support Center upon request.

2.2 Multicomputing

Chapter overview

Section	Description	Page
2.2.1	Peculiarities	2-5
2.2.2	Multicomputing Interrupt	2-6
2.2.3	Configuring and programming multicomputing operation	2-6

What is multicomputing?

Multicomputing refers to the concurrent operation of several (max. 4) CPUs which are capable of multicomputing in a central S7-400 system.

The participating CPUs automatically change their status in synchronism. That is, all CPUs are in synchronism during startup and transitions to STOP. Every CPU executes its own user program, irrespective of the user programs in the other CPUs. This feature facilitates the execution of control tasks in parallel.

Which racks are suitable for multicomputing?

The racks listed below are suitable for multicomputing:

- UR1 and UR 2
- UR2-H, multicomputing with several CPUs is only possible if all CPUs are inserted in the same in the same unit.
- CR3, the CR3 is equipped only with four slots, that is, you can only operate two CPUs in multicomputing mode.

Difference between multicomputing mode and operation in a segmented rack

The segmented rack CR2 (physically segmented, can not be configured in the software) allows only one CPU per segment. This, however, is not a multicomputing system. The CPUs in the segmented rack form an independent unit and respond in the same way as single-processor systems. A shared logical address space does not exist.

Hence, multicomputing is not possible in segmented racks (see also the installation manual).

When do I use multicomputing?

In the following situations it is of advantage to use multicomputing:

- The size of your user program exceeds the capacity of a single CPU and you run out of storage space: distribute program execution to several CPUs.
- A certain part of your system requires high-speed processing: cut the relevant program section from the program and process it on a separate "high-speed" CPU.
- Your system consists of several units which can be easily partitioned and controlled independently: Execute system partition 1 on CPU 1, system partition 2 on CPU 2, etc.

Example

The figure below shows a PLC operating in multicomputing mode. Each CPUs can access its assigned modules (FM, CP, SM).

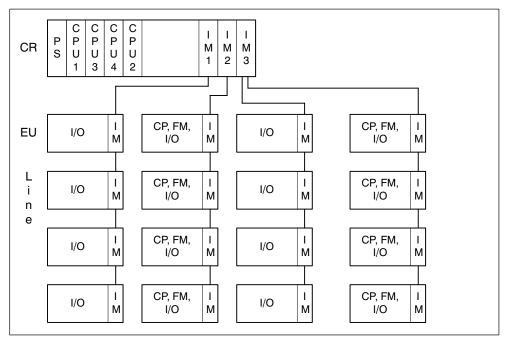


Figure 2-1 Multicomputing Example

2.2.1 Peculiarities

Slot Rules

In multicomputing operation, up to four CPUs can be inserted at the same time and in any order in a central controller (CC).

Bus Connection

The CPUs are interconnected via the communication bus (K bus). That is, if configured accordingly, all CPUs can be accessed by the PG via MPI interface.

Behavior at Startup and During Operation

During startup, all multicomputing CPUs automatically verify that they can operate in synchronism with each other. Synchronization is only possible if the requirements are satisfied:

- All configured CPUs (but only those) are inserted and fully functional.
- A proper configuration was created in STEP 7 and loaded to all CPUs in the rack.

If one of these conditions is not satisfied, an event with the ID 0x49A4 is output to the diagnostic buffer. For information on event IDs, refer to the reference help for standard and system functions.

When the CPU exits STOP mode, it compares the startup modes (COLD RESTART/RESTART (WARM RESTART) / HOT RESTART). With different startup modes, the CPUs do **not** switch to RUN mode.

Assignment of Addresses and Interrupts

In multicomputing mode, each CPU can access the modules it was assigned in the STEP 7 configuration. The address area of a module is always assigned exclusively to one CPU.

Each interrupt-capable module is therefore assigned to a CPU. Interrupts originating from such a module can not be received by the other CPUs.

Interrupt Processing

The following applies to interrupt processing:

- Process interrupts and diagnostic interrupts are only sent to one CPU.
- When a module fails or is removed or inserted, the interrupt is processed by the CPU that was assigned to the module in the STEP 7 configuration.
 Exception: A module insertion/removal interrupt output by a CP reaches all the CPUs, irrespective of the CP having been assigned to a CPU in the STEP 7 configuration.
- In the event of a rack failure, OB 86 is called on each CPU, including the CPUs which were not assigned a module in the faulty rack.

For further information on OB86, refer to the reference help on organization blocks.

I/O application specification

The typical I/O application specification of a PLC corresponds in multicomputing operation to the typical application specification of the CPU with the most resources. The relevant CPU-specific or DP master-specific typical application specifications cannot be exceeded in the individual CPUs.

2.2.2 Multicomputing Interrupt

Using the multicomputing interrupt (OB 60), you can respond synchronously to an event in multicomputing on the corresponding CPUs. In contrast to the process interrupts triggered by signal modules, the multicomputing interrupt can be output only by CPUs. The multicomputing interrupt is triggered by calling SFC 35 "MP ALM".

You will find more information in the *System Software for S7-300/400, System and Standard Functions* manual.

2.2.3 Configuring and programming multicomputing operation

Please refer to the manual *Configuring Hardware and Communication Connections with STEP 7* to find out how to configure and program the CPUs and the modules.

2.3 Modifications to the System During Operation

Certain changes can be made in the system configuration by means of CiR (Configuration in RUN) while the system is in RUN. Processing is halted for a brief period in order to accomplish this. The upper limit of this time period is set to one second by default but can be changed. During this time, the process inputs retain their most recent value (see the manual, *"Modifications to the System During Operation Using CiR"*

You can download a free copy of this manual from the Internet address:http://www.siemens.com/automation/service&support

You can modify the system during operation using CiR in system segments with distributed I/O. This requires a configuration as shown in the following illustration. To simplify the example, only one DP master system and one PA master system are shown. These restrictions do not apply in actual practice.

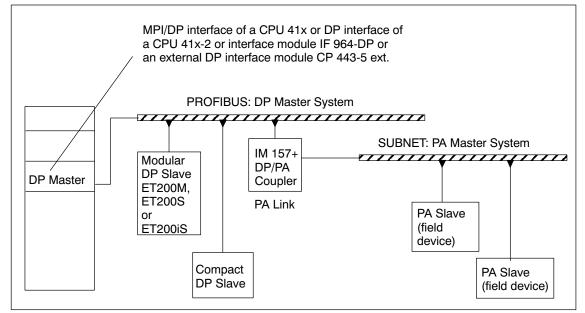


Figure 2-2 Overview: Architecture enabling modification of a system during operation

Hardware Requirements for Modification of a System During Operation

The following hardware requirements must have been fulfilled earlier in the commissioning phase in order to be able to subsequently modify the system during operation:

- An S7-400 standard CPU (CPU 412, CPU 414, CPU 416 or CPU 417), firmware V3.1 or later, or an S7-400-H-CPU (CPU 414-4H or CPU 417-4H) in single mode firmware V3.1 or later.
- If you wish to modify the system during operation on a DP master system with remote DP master (CP 443-5 extended), it must have firmware V5.0 or later.
- If you want to add modules for the ET 200M: Use the IM153-2 version MLFB 6ES7153-2AA03-0XB0 or later or the IM 153-2FO version MLFB 6ES7153-2BB00-0XB0 or later. You will also need to install the ET 200M with active bus elements and with enough free space for the planned expansion. You may not install the ET 200M as DPV0 slave (using a GSD file).
- If you wish to add entire stations: be sure to include the required bus connectors, repeaters, etc.
- If you wish to add PA slaves (field devices): use the IM157 version 6ES7157-0AA82-0XA00 or later in the corresponding DP/PA Link.
- The CR2 rack cannot be used.
- CP 444 and IM 467 modules can not be used within a station of which you want to modify the system configuation data in RUN by means of CiR.
- No multicomputing.
- No clocked operation on the same DP master system.

Note

You can freely mix components that are capable of system modification during operation and those that are not (except for the excluded modules, see above). However, you can modify the system configuration of components which are compatible with CiR.

Software Requirements for System Modifications During Operation

To be able to change a configuration in RUN mode, the user program must fulfill the following requirements: it must be written in such a way that station failures, module faults or exceeding cycle times do lead to a CPU STOP.

The following OBs are installed on the CPU:

- Process interrupt OBs (OB 40 to OB 47)
- Time-out error OB (OB 80)
- Diagnostic interrupt OB (OB 82)
- Insertion/removal OB (OB 83)
- CPU hardware error OB (OB 84)
- Runtime error OB (OB 85)
- Rack failure OB (OB 86)
- I/O access error OB (OB 122)

Permitted system modifications during operation: overview

The following modifications can be made to the system during operation:

- Add modules to the modular DP slave ET 200M, provided it has not been implemented as DPV0 slave (by means of GSD file)
- Reconfigure ET 200M modules, for example, modifying interrupt limits, or using the free channels.
- Use of the free channels of a module, or of a module of the ET 200M, ET 200S, ET 200iS modular slaves.
- Add DP slaves to an existing DP master system.
- Add PA slaves (field devices) to a PA master system
- Install DP/PA couplers downstream of an IM157
- Add PA Links (including PA master systems) to an existing DP master system
- Assign modules o a process image partition
- Reconfigure the modules of ET 200M stations (standard modules and fail-safe signal modules in standard mode).
- Undo modifications: for example, added modules, submodules, DP slaves and PA slaves (field devices) can be removed again.

Note

You can not add or remove slaves or modules, or make changes to a process image partition, on systems containing more than four DP masters.

Changes in RUN other than those specified earlier are not permitted and are excluded from this documentation.

Automation System S7-400 CPU Specifications A5E00267840-03

3

S7-400 in PROFIBUS DP mode

Chapter overview

In section	You find	On Page
3.1	CPU 41x as DP Master/DP Slave	3-2
3.2	Direct Communication	3-31
3.3	Consistent Data	3-34

3.1 CPU 41x as DP Master/DP Slave

Introduction

This section contains the properties and technical specifications you require for using a 41x CPU as DP master or DP slave and to configure these for direct data exchange.

Agreed is: Because of the fact that DP master / DP slave behavior is the same for all CPUs, we refer to the CPUs described below as 41x CPU.

Further reference material

For information on the HW and SW configuration of a PROFIBUS subnet and on diagnostics functions within the PROFIBUS subnet, refer to the *STEP 7* Online Help.

3.1.1 DP address areas of 41x CPUs

Address areas of 41x CPUs

Table 3-1	CPUs 41x	(MPI/DP Interface as PROFI	BUS DP)
-----------	----------	----------------------------	---------

Address area	412-1	412-2	414-2	416-2
MPI interface as PROFIBUS DP, of inputs and of outputs [bytes]	2048	2048	2048	2048
DP interface as PROFIBUS DP, of inputs and of outputs [bytes]	-	4096	6144	8192
Of those in the process image, of inputs and of outputs Setting with up to x bytes	4096	4096	8192	16384

Table 3-2 CPUs 41x (MPI/DP Interface and DP Module as PROFIBUS DP)

Address area	414-3	416-3	417-4
MPI interface as PROFIBUS DP, of inputs and of outputs [bytes]	2048	2048	2048
DP interface as PROFIBUS DP, of inputs and of outputs [bytes]	6144	8192	8192
DP module as PROFIBUS DP, of inputs and of outputs [bytes]	6144	8192	8192
In the process image, of inputs and of outputs Setting with up to x bytes	8192	16384	16384

In the input address area, the **DP diagnostic addresses** occupy at least one byte for the DP master and each DP slave. The DP standard diagnosis for each node can be called at these addresses, for example (LADDR parameter of SFC 13). You define the DP diagnostic addresses in the configuration data, otherwise *STEP 7* assigns these automatically as DP diagnostic addresses in ascending order, starting at the highest byte address.

For DPV1 master mode, the slaves are usually assigned two diagnostic addresses.

3.1.2 41x CPU as PROFIBUS DP master

Introduction

This section provides information on the properties and technical data of a CPU operating in DP master mode.

Starting with section 6.1, you can find this information for 41x CPUs.

Requirements

You must configure the relevant CPU interface for operation in DP master mode. That is, in *STEP 7* you

- Configure the CPU as DP master
- Assign a PROFIBUS address
- Select an operating mode (S7-compatible or DPV1)
- Assign a diagnostic address
- Connect DP slaves to the DP master system

Note

Is one of the PROFIBUS DP slaves a 31x or 41x CPU?

If yes, you will find it in the PROFIBUS DP catalog as a "preconfigured station". Assign this DP slave CPU a slave diagnostic address in the DP master. Interconnect the DP master with the DP slave, and define the address areas for data exchange with the DP slave.

From EN 50170 to DPV1 standard

The enhancements of the EN 50170 standard for distributed I/O were incorporated in IEC 61158 / IEC 61784-1:2002 Ed1 CP 3/1. The SIMATIC documentation refers to these as DPV1. The new version features a few additions and simplifications.

This DPV1 functionality is already implemented on certain SIEMENS automation components. Some slight modifications are required in order to enable this new functionality for your system. Information on the migration from EN 50170 to DPV1 is available on the Internet, on the FAQ pages "Changing from EN 50170 to DPV1", FAQ ID 7027576, of the Customer Support.

Components supporting PROFIBUS DPV1 functionality

DPV1 masters

- S7-400 CPUs with integrated DP interface, with firmware V3.0 or higher.
- CP 443-5, order number 6GK7443-5DX03-0XE0, if used with one of these S7-400 CPUs.

DPV1 slaves

- DP slaves listed under their family name in the STEP 7 hardware catalog can be identified as DPV1 slave based on the included comment.
- DP slaves integrated in STEP 7 by means of GSD files, GSD Rev. 3 or higher.

STEP 7

STEP 7 V5.1 with Service Pack 2, or a higher version.

What are the operating modes for DPV1 components?

• S7-compatible

In this mode, the components are compatible to EN 50170. Note that you can not utilize the full DPV1 functionality in this mode.

DPV1 mode

In this mode, you can utilize the full DPV1 functionality. Incompatible automation components in the station can be used as before.

DPV1 and EN 50170 compatibility

You can continue to use all existing slaves after the system conversion to DPV1. These are, however, do not support the enhanced function of DPV1.

DPV1 slaves can be implemented in system which are not converted to DPV1. In this case, their behavior corresponds with that of conventional slaves. SIEMENS DPV1 slaves can be operated in S7-compatible mode. For the DPV1 slaves of external manufacturers, you need a GSD file < Rev. 3 file to EN50170.

Migrating to DPV1

The migration to DPV1 applies to the entire station. You can set this DP mode in HW Config in STEP 7.

Further Information

Descriptions and information relating to the migration from PROFIBUS DP to PROFIBUS DPV1 is found on the Internet URL:

http://www.siemens.com/automation/service&support

Refer to ID 7027576

Monitor / modify, programming via PROFIBUS

The PROFIBUS DP interface is an alternative to the MPI interface you can use to program the CPU or execute the PG functions Monitor and Modify.

Note

The execution of programming and monitor/modify functions via PROFIBUS DP interface prolongs the DP cycle.

Constant bus cycle time

This is a property of PROFIBUS DP. The "Constant bus cycle time" function ensures that the DP master always starts the DP bus cycle within a constant interval. From the view of the slaves, this means that they receive their data from the master at constant time intervals.

In STEP 7 V 5.2 or higher, you can configure constant bus cycle times for PROFIBUS subnets.

Clocked update of process image partitions

SFC 126 "SYNC_PI" is used for the clocked update of the process image partition of inputs. An application program which is interconnected to a DP cycle can use the SFC for consistent updates of the data recorded in the process image partition of inputs in synchronism with this cycle. SFC126 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

SFC 127 "SYNC_PO" s used for the clocked update of the process image partition of ouptuts. An application program which is interconnected to a DP cycle can use the SFC for the consistent transfer of the computed output data of a process image partition of outputs to the I/O in synchonism with this cycle. SFC127 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

To allow clocked updates of process image partitions, all input or output addresses of a slave must be assigned to the same process image partition.

To ensure consistency of data in a process image partition, the following conditions must be satisfied on the various CPUs:

- CPU 412: number of slaves + number of bytes / 100 < 16
- CPU 414: number of slaves + number of bytes / 100 < 26
- CPU 416: number of slaves + number of bytes / 100 < 40
- CPU 417: number of slaves + number of bytes / 100 < 44

The SFCs 126 and 127 are descibed in the corresponding Online Help and in the "System and Standard Functions" manual.

Consistent user data

These are data which are associated in context and describe a process status at a given time. To ensure consistency, these data should not be modified or updated while being processed or transferred.

For details, refer to chapter 3.3.

SYNC/FREEZE

The SYNC control command is used to set sync mode at the DP slaves of selected groups. That is, the DP master transfers current output data and instructs the relevant DP slaves to freeze their outputs. The DP slaves writes the output data of the next output datagrams to an internal buffer; the state of the outputs remains unchanged.

Following each SYNC control command, the DP slaves of the selected groups transfer the output data stored in the internal buffer to the process outputs.

The outputs are only updated cyclically again after you transfer the UNSYNC control command using SFC 11 "DPSYC_FR".

The FREEZE control command is used to set the relavant DP slaves to Freeze mode, that is, the DP master instructs the DP slaves to freeze the current state of the inputs. It then transfers the frozen data to the input area of the CPU.

Following each FREEZE control command, the DP slaves freeze the state of their inputs again.

The DP master receives the current state of the inputs cyclically again not until you have sent the UNFREEZE control command with SFC 11 "DPSYC FR".

For information on SFC 11, refer to the corresponding Online Help or to the "System and Standard Functions" manual.

Power-up of the DP master system

Use the following parameters to set power-up monitoring of the DP master:

- Transfer of the parameters to modules
- "Ready" message from the module

In other words, the DP slaves must power up and be configured by the CPU (as DP master) within the set time.

PROFIBUS Address of the DP Master

All PROFIBUS addresses are allowed.

3.1.3 Diagnostics of the CPU 41x as DP Master

Diagnostics Using LEDs

Table 3-3 explains the meaning of the BUSF LED. The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 3-3	Meaning of the BUSF LED of the CPU 41x as DP Master
10010 0 0	

BUSF	Meaning	What to Do
Off	Configuration correct	-
	All configured slaves can be addressed	
Lit	Bus fault (hardware fault)	• Check for short-circuit or interruption of the bus cable.
	DP interface fault	Analyze the diagnosistic data.
	Different transmission rates in multi-DP master mode	Reconfigure or correct the configuration.
Flashing	Station failure	• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted.
	 At least one of the assigned slaves can not be addressed 	• Wait until the CPU 41x has powered up. If the LED does not stop flashing, check the DP slaves or analyze the diagnosistic data of the DP slaves.
Flashes briefly INTF lights up briefly	CiR synchronization running	_

Initiating the detection of the Bus Topology in a DP Master System using SFC 103 "DP_TOPOL"

The diagnostics repeater is provided to enhance the options of locating faulty modules or DP cable interruptions when runtime errors have occurred. This module operates as a slave and can determine the topology of a DP slave and record any errors based on this information.

SFC 103 "DP_TOPOL" is used to initiate the detection of the bus topology of a DP master systems by means of the diagnostics repeater. SFC 103 is described in the corresponding Online Help and in the "System and Standard Functions" manual. For information on the diagnostics repeater, refer to the "Diagnostics Repeater for PROFIBUS DP" manual, order number 6ES7972-0AB00-8BA0.

Reading diagnosistic data in STEP 7

DP Master	Block or Tab in STEP 7	Application	Refer To
CPU 41x	DP slave diagnostics tab	To display the slave diagnosis as plain text at the <i>STEP 7</i> user interface	See the section on hardware diagnostics in the <i>STEP 7</i> online help system and the <i>STEP 7</i> user guide
	SFC 13 "DPNRM_DG"	To read out the slave diagnosis (store in the data area of the user program)	For info on the structure of CPU 41x, see Section 3.1.5; SFC see the reference manual <i>System and Standard Functions</i> For info on the structure for other slaves, refer to the relevant sections
	SFC 59 "RD_REC"	To read out data records of the S7 diagnosis (store the data in the data area of the user program)	
	SFC 51 "RDSYSST"	To read out SSL sublists. Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	
	SFB 52 "RDREC"	For DPV1 slaves: To read out data records of the S7 diagnosis (store in the data area of the user program)	Reference Manual System and Standard Functions
	SFB 54 "RALRM"	For DPV1 slaves:	
		To read out interrupt information within the associated interrupt OB	
	SFC 103 "DP_TOPOL"	Triggers detection of the bus topology of a DP master system with diagnostic repeaters installed there.	

 Table 3-4
 Reading Out the Diagnosis with STEP 7

Analysis of diagnosistic data in the user program

The following figure shows you how to evaluate the diagnosis in the user program.

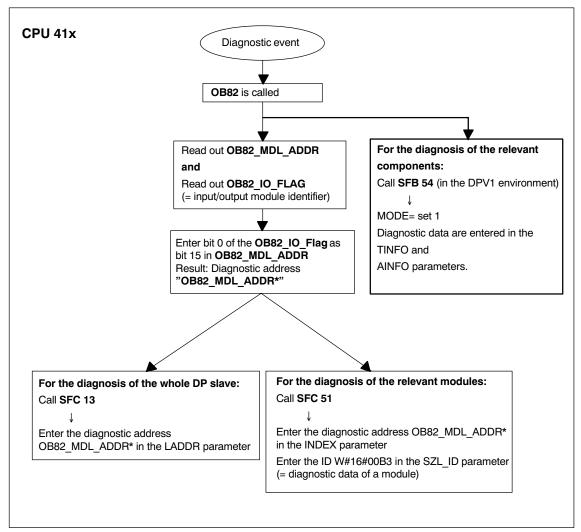


Figure 3-1 Diagnostics with CPU 41x

Diagnostic Addresses in Connection with DP Slave Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

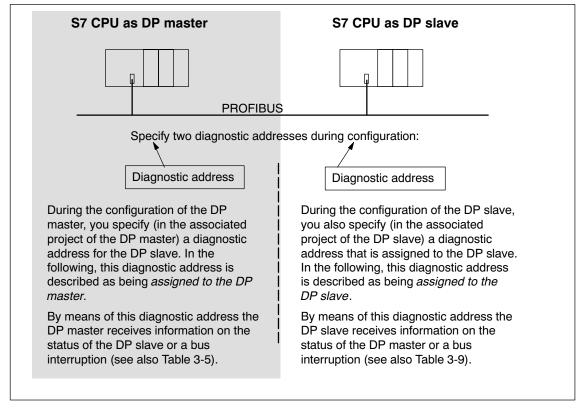


Figure 3-2 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 3-5 shows you how the CPU 41x as DP master detects any changes in the operating mode of a CPU as DP slave or interruptions in data transfer.

Table 3-5	Event Detection of the CPUs 41x as DP Master

Event	What Happens in the DP Master
Bus interruption (short circuit, connector removed)	 OB 86 called with the message Station failure (incoming event; diagnostic address of the DP slave that is assigned to the DP master) In the case of I/O access: OB 122 called (I/O access error)
DP slave: RUN \rightarrow STOP	 OB 82 is called with the message Faulty module (incoming event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=1)
DP slave: STOP \rightarrow RUN	 OB 82 is called with the message <i>Module OK</i>. (outgoing event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table shows you how, for example, you can evaluate RUN-STOP transitions of the DP slave in the DP master (see also Table 3-5).

In the DP Master	In the DP Slave (CPU 41x)
Diagnostic addresses: (example) Master diagnostic address=1023 Slave diagnostic address in the master system=1022	Diagnostic addresses: (example) Slave diagnostic address= 422 Master diagnostic address=not relevant
The CPU calls OB 82 with the following	$ CPU: RUN \rightarrow STOP$
information, amongst other things:	CPU generates a DP slave diagnostic frame .
 OB 82_MDL_ADDR:=1022 OB82_EV_CLASS:=B#16#39 (incoming event) 	
OB82_MDL_DEFECT:=module malfunction	
Tip: This information is also in the diagnostic buffer of the CPU	
You should also program the SFC 13 "DPNRM_DG" in the user program to read out the DP slave diagnostic data.	
We recommend you use SFB 54 in the DPV1 environment. It outputs the interrupt information in its entirety.	

3.1.4 CPU 41x as DP Slave

Introduction

In this section we describe the features and technical specifications of the CPU if you operate it as a DP slave.

You can find the features and technical specifications of the CPUs 41x as of Section 6.1.

Requirements

- 1. Only one DP interface of a CPU can be configured as a DP slave.
- 2. Is the MPI/DP interface to be a DP interface? If so, you must configure the interface as a DP interface.

Before commissioning you must configure the CPU as a DP slave. In other words, you must do the following in STEP 7 $\,$

- Activate the CPU as a DP slave
- Assign a PROFIBUS address
- Assign a slave diagnostic address
- Define the address areas for data transfer to the DP master

GSD Files

You need a DDB file to configure the CPU as a DP slave in a third-party system.

You can download the GSD file free of charge from the Internet at http://www.ad.siemens.de/csi_e/gsd.

You can also download the GSD file from the mailbox of the Interface Center in Fürth on +49 (911) 737972.

Configuration and Parameter Assignment Frame

When you configure and assign parameters to CPU 41x, you are supported by *STEP 7*. If you require a description of the configuration and parameter assignment frame to carry out a check with a bus monitor, for example, you will find it on the Internet at http://www.ad.siemens.de/simatic-cs under the ID 1452338

Monitor/Modify, Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify. To do this, you must enable these functions when you configure the CPU as DP slave in *STEP 7*.

Note

The use of Programming or Monitor and Modify via the PROFIBUS DP interface extends the DP cycle.

Data Transfer Via an Intermediate Memory

As a DP slave the CPU 41x makes an intermediate memory available to PROFIBUS DP. Data transfer between the CPU as DP slave and the DP master always takes place via this intermediate memory. You can configure up to 32 address areas for this.

In other words, the DP master writes its data in these address areas of the intermediate memory and the CPU reads the data in the user program and vice versa.

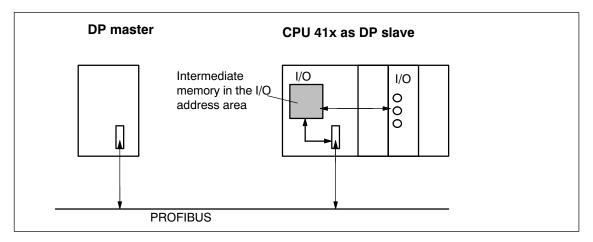


Figure 3-3 Intermediate Memory in the CPU 41x as DP Slave

Address Areas of the Intermediate Memory

Configure in STEP 7 the input and output address areas:

- You can configure up to 32 input and output address areas.
- Each of these address areas can be up to 32 bytes in size
- You can configure a maximum of 244 bytes of inputs and 244 bytes of outputs in total

An example for the configuration of the address assignments of the intermediate memory is provided in the table below. You will also find this in the online help for STEP 7 configuration.

Table 3-6 Configuration Example for the Address Areas of the Intermediate Memory

	Туре	Master Address	Туре	Slave Address	Length	Unit	Consistency
1	е	222	A	310	2	Byte	Unit
2	Α	0	е	13	10	Word	Total length
:							
32							
	Address areas in the DP master CPU		Address slave C	s areas in the DP PU	areas mu	rameters of the st be the same nd DP slave	

Rules

You must adhere to the following rules when working with the intermediate memory:

- Assignment of the address areas:
 - Input data of the DP slave are always output data of the DP master
 - Output data of the DP slave are always input data of the DP master
- You can assign the addresses as you choose. You access the data in the user program with load/transfer commands or with SFCs 14 and 15. You can also specify addresses from the process image input and output table (see also section 3.1.1).

Note

You assign addresses for the intermediate memory from the DP address area of the CPU 41x.

You must not reassign the addresses you have already assigned to the intermediate memory to the I/O modules on the CPU 41x.

- The lowest address in each address area is the start address of that address area.
- The length, unit and consistency of address areas for the DP master and DP slave that belong together must be the same.

S5 DP Master

If you use an IM 308 C as a DP master and the CPU 41x as a DP slave, the following applies to the exchange of consistent data:

You must program FB 192 in the IM 308-C so that consistent data can be transferred between the DP master and DP slave. The data of the CPU 41x are only output or displayed contiguously in a block with FB 192.

S5-95 as DP Master

If you use an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 41x as DP slave.

Sample Program

The small sample program below illustrates data transfer between the DP master and DP slave. This example contains the addresses from Table 3-6.

	In the DP Slave CPU				In	the DP M	laster CPU
L	2		Preprocess data				
т	MB	6	in the DP slave				
L	EB	0					
т	MB	7					
L	MW	6	Transfer data to				
т	PQW	310	the DP master				
				L	PIB	222	Continue to
				т	MB	50	process received
				L	PIB	223	data in the DP
				L	B#16#3		master
				+	I		
				т	MB	51	
				L	10		Preprocess data
				+	3		in the DP master
				т	MB	60	
				CALL	SFC	15	Send data to the
				LADDI	R:= W#16#	0	DP slave
				RECOR	RD:= P#M6	0.0 Byte	e20
				RET_V	VAL:= MW	22	
CALL	SFC	14	Receive data				
LADD	R:=W#16#	D	from the DP				
RET	RET VAL:=MW 20 master						
RECO	RD:=P#M3	80.0 Byte20	1				
L	MB	30	Continue to				
L	MB	7	process received				
+	I		data				
т	MW	100					

Data Transfer in STOP Mode

The DP slave CPU goes into STOP mode: The data in the intermediate memory of the CPU are overwritten with "0". In other words, the DP master reads "0".

The DP master goes into STOP mode: The current data in the intermediate memory of the CPU are retained and can continue to be read by the CPU.

PROFIBUS Address

You cannot set 126 as PROFIBUS address for the CPU 41x as DP slave.

3.1.5 Diagnostics of the CPU 41x as DP Slave

Diagnostics using LEDs – CPU 41x

Table 3-7 explains the meaning of the BUSF LEDs. The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 3-7 Meaning of the BUSF LEDs of the CPU 41x as DP Slave

BUSF	Meaning	What to Do
Off	Configuration correct	-
Flashing	 The CPU 41x is incorrectly configured. There is no data interchange between the DP master and the CPU 41x. Causes: The response monitoring time has expired. Bus communication via PROFIBUS DP has been interrupted. The PROFIBUS address is incorrect. 	 Check the CPU 41x. Check to make sure that the bus connector is properly inserted. Check whether the bus cable to the DP master has been interrupted. Check the configuration and parameter assignment.
On	Bus short circuit	Check the bus setup.

Triggering Detection of the Bus Topology in a DP Master System with the SFC 103 "DP_TOPOL"

The diagnostics repeater is provided to improve the ability to locate disrupted modules or an interruption on the DP cables when failures occur in ongoing operation. This module operates as a slave and can determine the topology of a DP strand and record any faults originating from it.

You can use SFC 103 "DP_TOPOL" to trigger the analysis of the bus topology of a DP master systems by the diagnostics repeater. SFC 103 is documented in the corresponding online help and in the manual "System and Standard Functions". The diagnostics repeater is documented in the manual "Diagnostics Repeater for PROFIBUS DP", order number 6ES7972-0AB00-8BA0.

Diagnostics with STEP 5 or STEP 7 Slave Diagnostics

The slave diagnosis complies with the EN 50170, Volume 2, PROFIBUS standard. Depending on the DP master, it can be read out with *STEP 5* or *STEP 7* for all DP slaves that comply with the standard.

The display and structure of the slave diagnosis is described in the following sections.

S7 Diagnosis

An S7 diagnosis can be requested for all diagnostics-capable modules in the SIMATIC S7/M7 range of modules in the user program. You can find out which modules have diagnostic capability in the module information or in the catalog. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current status of a module. Data record 1 also contains module-specific diagnostic data.

You will find the structure of the diagnostic data described in the *Standard and System Functions* Reference Manual.

Reading Out the Diagnosis

Automation System with DP Master	Block or Tab in STEP 7	Application	Refer To
SIMATIC S7/M7	DP slave diagnostics tab	To display the slave diagnosis as plain text at the <i>STEP 7</i> user interface	See the section on hardware diagnostics in the STEP 7 online help system and in the STEP 7 user guide
	SFC 13 "DP NRM_DG"	To read out the slave diagnosis (store in the data area of the user program)	SFC see Reference Manual System and Standard Functions
	SFC 51 "RDSYSST"	To read out SSL sublists Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	See the <i>System and</i> <i>Standard Functions</i> Reference Manual
	SFB 54 "RDREC"	Applies to the DPV1 environment: To read out interrupt information within the associated interrupt OB	
	FB 125/FC 125	To evaluate slave diagnosis	The Internet page http://www.ad.siemens.de/ simatic-cs ID 387 257
SIMATIC S5 with IM 308-C as DP master	FB 192 "IM308C"	To read out the slave diagnosis (store in the data area of	FBs see the <i>ET 200</i> Distributed I/O System manual
SIMATIC S5 with S5-95U programmable controller as DP master	SFB 230 "S_DIAG"	the user program)	

Table 3-8 Reading Out the Diagnostic Data with STEP 5 and STEP 7 in the Master System

Example of Reading Out the Slave Diagnosis with FB 192 "IM 308C"

Here you will find an example of how to use FB 192 to read out the slave diagnosis for a DP slave in the *STEP 5* user program.

Assumptions

The following assumptions apply to this STEP 5 user program:

- The IM 308-C is assigned pages 0 to 15 (number 0 of the IM 308-C) as the DP master.
- The DP slave has the PROFIBUS address 3.
- The slave diagnosis is to be stored in DB 20. However, you can also use any other data block for this.
- The slave diagnosis consists of 26 bytes.

STEP 5 User Program

STL			Explanation
	:A	DB 30	
	:JU	FB 192	
Name	:IM30	8C	
DPAD	:	KH F800	Default address area of the IM 308-C
IMST	:	КҮ О, З	IM no. = 0, PROFIBUS address of DP slave = 3
FCT	:	KC SD	Function: Read slave diagnosis
GCGR	:	КМ О	Not evaluated
TYP	:	КҮ 0, 20	S5 data area: DB 20
STAD	:	KF +1	Diagnostic data from data word 1
LENG	:	KF 26	Length of diagnosis = 26 bytes
ERR	:	DW O	Error code stored in DW 0 of DB 30

Diagnostic Addresses in Connection with DP Master Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

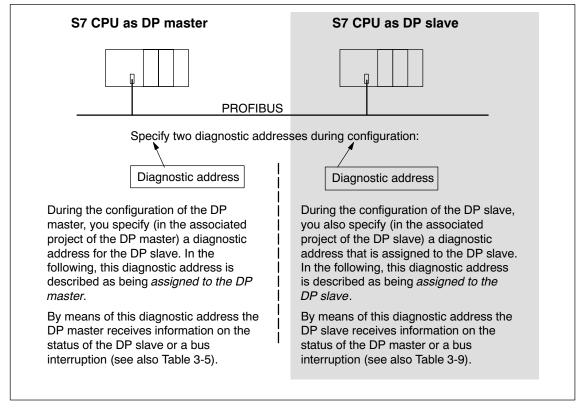


Figure 3-4 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 3-9 shows you how the CPU 41x as DP slave detects any operating mode changes or interruptions in data transfer.

Table 3-9	Event Detection of the CPUs 41x as DP Slave

Event	What Happens in the DP Slave
Bus interruption (short circuit, connector removed)	 OB 86 is called with the message <i>Station failure</i> (incoming event; diagnostic address of the DP slave that is assigned to the DP slave) In the case of I/O access: OB 122 called (I/O access error)
DP master: RUN \rightarrow STOP	 OB 82 is called with the message <i>Faulty module</i> (incoming event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=1)
DP master: STOP \rightarrow RUN	 OB 82 is called with the message <i>Module OK</i>. (outgoing event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table 3-10 shows you, for example, how you can evaluate RUN-STOP transitions of the DP master in the DP slave (see also Table 3-9).

Table 3-10 Evaluation of RUN-STOP Transitions in the DP Master/DP Slave

In the DP Master	In the DP Slave
Diagnostic addresses: (example) Master diagnostic address= 1023 Slave diagnostic address in the master system= 1022	Diagnostic addresses: (example) Slave diagnostic address= 422 Master diagnostic address=not relevant
CPU: RUN → STOP	 The CPU calls OB 82 with the following information, amongst other things: OB 82_MDL_ADDR:=422 OB82_EV_CLASS:=B#16#39 (incoming event) OB82_MDL_DEFECT:=module malfunction
	Tip: This information is also in the diagnostic buffer of the CPU

Structure of the Slave Diagnosis

Byte 0 Byte 1 Byte 2		Station states 1 to 3
Byte 3		Master PROFIBUS Address
Byte 4 Byte 5		High-Order Byte Low byte
Byte 6 to Byte x	- - -	Module Diagnosis (The length depends on the number of configured address areas in the intermediate memory ¹)
Byte x+1 to Byte y	· · · · · · · · · · · · · · · · · · ·	Station Diagnosis (The length depends on the number of configured address areas in the intermediate memory)
	n: In the case of invalid co interpretes 35 configured	onfiguration of the DP master, the I address areas (46 _H).

Figure 3-5 Structure of the Slave Diagnosis

3.1.6 CPU 41x as DP slave: Station States 1 to 3

Station states 1 to 3

Station status 1 to 3 provides an overview of the status of a DP slave.

Bit	Meaning	What to Do
0	1: The DP slave cannot be addressed by the DP master.	 Correct DP address set on the DP slave? Bus connector connected? Voltage on DP slave? RS 485 repeater set correctly? Execute reset on the DP slave
1	1: The DP slave is not yet ready for data transfer.	Wait while the DP slave powers up.
2	1: The configuration data sent by the DP master to the DP slave does not correspond to the actual configuration of the DP slave.	 Correct station type or correct configuration of the DP slave entered in the software?
3	 Diagnostic interrupt, triggered by RUN-STOP transition of the CPU Diagnostic interrupt, triggered by STOP-RUN transition of the CPU 	You can read out the diagnosis.
4	1:Function is not supported, e.g. changing the DP address via software	Check the configuration.
5	0: The bit is always "0".	-
6	1: The DP slave type does not correspond to the software configuration.	Correct station type entered in the software? (Parameter assignment error)
7	1: Parameters have been assigned to the DP slave by a different DP master to the one that currently has access to the DP slave.	 Bit is always at 1, when you are accessing the DP slave using the programming device or another DP master, for example. The DP address of the parameter assignment master is in the "master PROFIBUS address" diagnostic byte.

Table 3-11	Structure of the Station Status 1 (E	svte 0)
		yic 0)

Table 3-12 Structure of Station Status 2 (Byte 1)

Bit	Meaning			
0	1: The DP slave must be assigned new parameters and reconfigured.			
1	1: A diagnostic message has been issued. The DP slave cannot continue until the problem has been corrected (static diagnostic message).			
2	1: The bit is always set to "1" if the DP slave with this DP address is present.			
3	1: Response monitoring is enabled for this DP slave.			
4	0: The bit is always at "0".			
5	0: The bit is always at "0".			
6	0: The bit is always at "0".			
7	1: The DP slave is disabled – that is, it has been removed from cyclic processing.			

Table 3-13 Structure of Station Status 3 (Byte 2)

Bit	Meaning						
0							
to	0: The bits are always at "0".						
6							
7	1:	٠	There are more diagnostic messages than the DP slave can store.				
		•	The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.				

Master PROFIBUS Address

The master PROFIBUS address diagnostic byte contains the DP address of the DP master that:

- assigns parameters for the DP slave and
- · has read and write access to the DP slave

Table 3-14 Structure of the Master PROFIBUS Address (Byte 3)

Bit	Meaning
0 to 7	DP address of the DP master which configured the DP slave and which has read and write access to the DP slave.
	FF _H : DP slave has not been configured by any DP master.

Manufacturer ID

The manufacturer ID contains a code that describes the type of DP slave.

Byte 4	Byte 5	Manufacturer ID for CPU
80 _H	C5 _H	412-1
80 _H	C6 _H	412-2
80 _H	C7 _H	414-2
80 _H	C8 _H	414-3
80 _H	CA _H	416-2
80 _H	CBH	416-3
80 _H	CCH	417-4

Table 3-15 Structure of the Manufacturer ID (Bytes 4, 5)

Module Diagnosis

The module diagnosis tells you for which of the configured address areas of the intermediate memory an entry has been made.

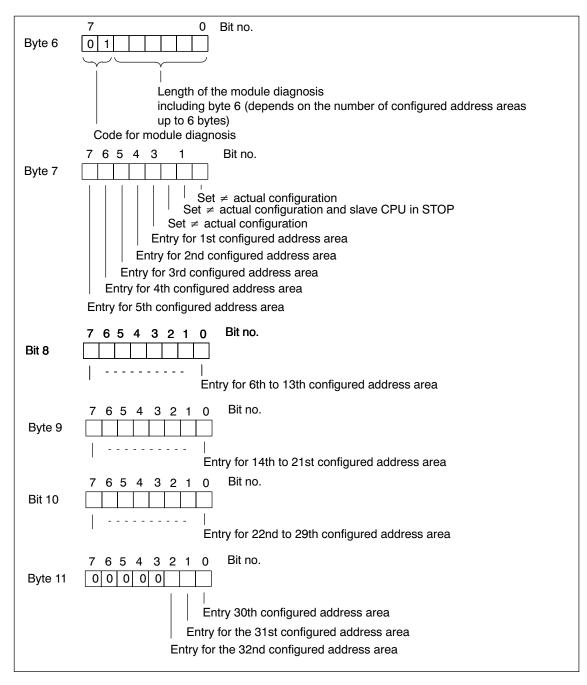


Figure 3-6 Structure of the Module Diagnosis of the CPU 41x

Station Diagnosis

The station diagnosis provides detailed information on a DP slave. The station diagnosis starts as of byte x and can include up to 20 bytes.

The figure below illustrates the structure and contents of the bytes for a configured address area of the intermediate memory.

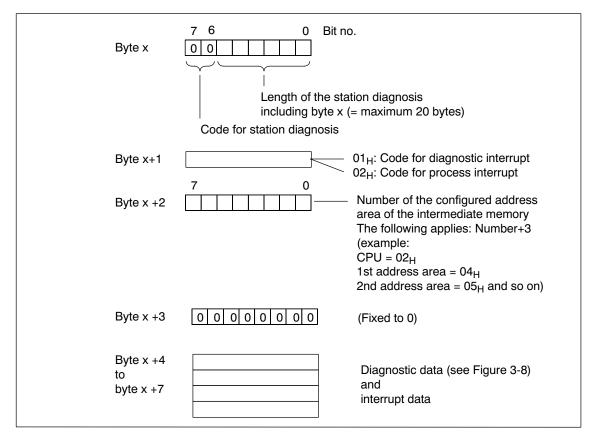


Figure 3-7 Structure of the Station Diagnosis

As of byte x +4

The meaning of the bytes as of byte x+4 depends on byte x +1 (see Figure 3-7).

In Byte x +1, the Code Stands for:			
Diagnostic Interrupt (01 _H)	Process Interrupt (02 _H)		
The diagnostic data contain the 16 byte status information of the CPU. Figure 3-8 shows you the assignment of the first 4 bytes of the diagnostic data. The following 12 bytes are always 0.	You can program 4 bytes of interrupt information any way you wish for the process interrupt. You transfer these 4 bytes to the DP master in <i>STEP 7</i> using SFC 7 "DP_PRAL".		

Bytes x+4 to x+7 for Diagnostic Interrupts

Figure 3-8 illustrates the structure and contents of bytes x + 4 to x + 7 for the diagnostic interrupt. The contents of these bytes correspond to the contents of data record 0 of the diagnosis in *STEP 7* (in this case not all the bits are assigned).

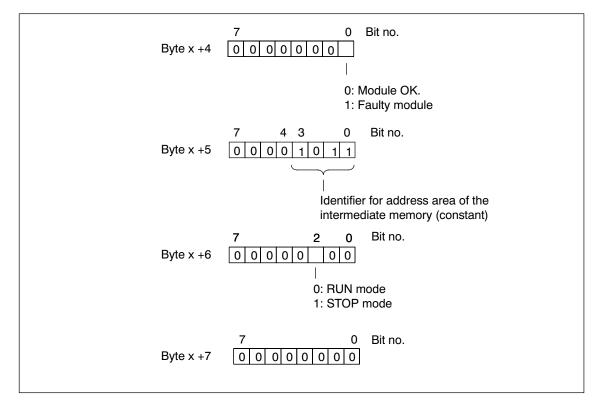


Figure 3-8 Bytes +4 to +7 for Diagnostic and Process Interrupts

Interrupts with the S7/M7 DP Master

In the CPU 41x as a DP slave you can trigger a process interrupt in the DP master from the user program. You can trigger an OB 40 in the user program of the DP master by calling SFC 7 "DP_PRAL". Using SFC 7 you can forward interrupt information in a double word to the DP master, which you can evaluate in OB 40 in the OB40_POINT_ADDR variable. You can program the interrupt information as you choose. You will find a detailed description of SFC 7 "DP_PRAL" in the *System Software for S7-300/400, System and Standard Functions* Reference Manual.

Interrupts with another DP Master

If you are running the CPU 41x with another DP master, these interrupts are reflected in the station diagnosis of the CPU 41x. You have to process the relevant diagnostic events in the DP master's user program.

Note

Note the following in order to be able to evaluate diagnostic interrupts and process interrupts by means of the station diagnosis when using a different DP master:

- The DP master should be able to store the diagnostic messages; in other words, the diagnostic messages should be stored in a ring buffer in the DP master. There are more diagnostic messages than the DP master can store, only the last diagnostic message received would be available for evaluation, for example.
- You must query the relevant bits in the station diagnosis at regular intervals in your user program. You must also take the PROFIBUS DP bus cycle time into consideration so that you can query the bits at least once synchronously with the bus cycle time, for example.
- You cannot use process interrupts in the station diagnosis with an IM 308-C as the DP master, because only incoming – and not outgoing – interrupts are reported.

3.2 Direct Communication

You can configure direct communication for PROFIBUS nodes as of *STEP 7* V 5.0. The CPU 41x can participate in direct communication as the sender or recipient.

"Direct Communication" represents a special type of communication relationship between PROFIBUS DP nodes.

3.2.1 Principle of Direct Data

Direct communication is characterized by the fact that PROFIBUS DP nodes "listen in" to find out which data a DP slave is sending back to its DP master. By means of this mechanism the "eavesdropper" (recipient) can access changes to the input data of remote DP slaves directly.

During configuration in *STEP 7*, you specify by means of the relevant I/O input addresses the address area of the recipient to which the required data of the sender are to be read.

A CPU 41x can be: Sender as a DP slave Recipient as a DP slave or a DP master or as a CPU that is not integrated in a master system (see Figure 3-9).

Example

Figure 3-9 uses an example to illustrate which direct communication "relationships" you can configure. All the DP masters and DP slaves in the figure are CPUs 41x. Note that other DP slaves (ET 200M, ET 200X, ET 200S) can only be senders.

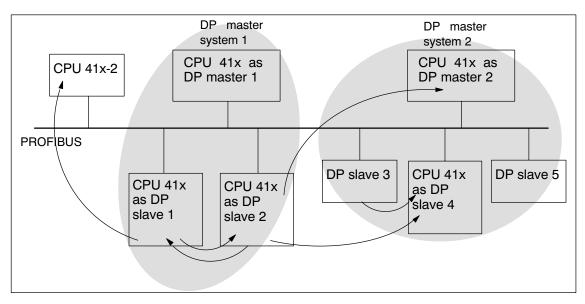


Figure 3-9 Direct Communication with CPUs 41x

3.2.2 Diagnostics in Direct Communication

Diagnostic Addresses

In direct communication you assign a diagnostic address in the recipient:

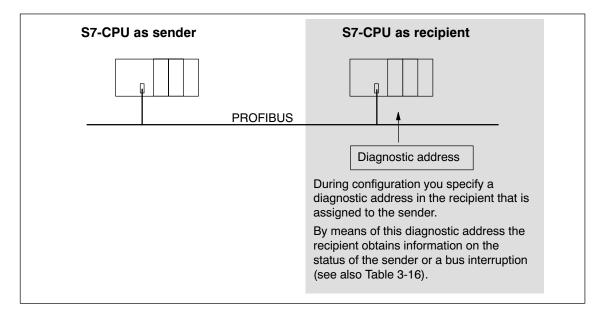


Figure 3-10 Diagnostic Address for the Recipient During Direct Communication

Event Detection

Table 3-16 shows you how the CPU 41x as recipient detects interruptions in data transfer.

 Table 3-16
 Event Detection of the CPUs 41x as Recipient During Direct Communication

Event	What Happens in the Recipient			
Bus interruption (short circuit, connector removed)	 OB 86 is called with the message Station failure (incoming event; diagnostic address of the recipient assigned to the sender) 			
	 In the case of I/O access: OB 122 called (I/O access error) 			

Evaluation in the User Program

The following table 3-17 shows you, for example, how you can evaluate a sender station failure in the recipient (see also Table 3-16).

Table 3-17 Evaluation of the Station Failure in the Sender During Direct Communication

In the Sender	In the Recipient
Diagnostic addresses: (example) Master diagnostic address=1023 Slave diagnostic address in the master system=1022	Diagnostic address: (example) Diagnostic address =444
Station failure	 The CPU calls OB 86 with the following information, amongst other things: OB 86_MDL_ADDR:=444 OB86_EV_CLASS:=B#16#38 (incoming event) OB86_FLT_ID:=B#16#C4 (failure of a DP station)
	Tip: This information is also in the diagnostic buffer of the CPU

3.3 Consistent Data

Data that belongs together in terms of its content and a process state written at a specific point in time is known as consistent data. To maintain consistency, the data should not be changed or updated during processing or transmission.

Example

To ensure that the CPU has a consistent image of the process signals for the duration of cyclic program scanning, the process signals are read from the process image inputs prior to program scanning and written to the process image outputs after the program scanning. Subsequently, during program scanning when the address area "inputs" (I) and "outputs" (O) are addressed, the user program addresses the internal memory area of the CPU on which the image of the inputs and outputs is located instead of directly accessing the signal modules.

SFC 81 "UBLKMOV"

With SFC 81 "UBLKMOV" (uninterruptible block move), you can copy the contents of a memory area (= source area) consistently to a different memory area (= destination area). The copy operation cannot be interrupted by other operating system activities.

SFC 81 "UBLKMOV" enables you to copy the following memory areas:

- Memory markers
- DB contents
- Process image of the inputs
- Process image of outputs

The maximum amount of data you can copy is 512 bytes. Take into consideration the restrictions for the specific CPU, which are documented in the operations list, for example.

Since copying cannot be interrupted, the interrupt reaction times of your CPU may increase when using SFC 81 "UBLKMOV".

The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies as much data to the destination area as that contained in the source area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

For information on SFC 81, refer to the corresponding Online Help and to the *"System and Standard Functions"* manual.

3.3.1 Consistency for Communication Blocks and Functions

Using S7-400 the communication data is not processed in the scan cycle checkpoint; instead, this data is processed in fixed time slices during the program cycle.

In the system the byte, word and double word data formats can always be processed consistently, in other words, the transfer or processing of 1 byte, 1 word (= 2 bytes) or 1 double word (= 4 bytes) cannot be interrupted.

If communication blocks (such as SFB 12 "BSEND") are called in the user program, which are only used in pairs (such as SFB 12 "BSEND" und SFB 13 "BRCV") and which share access to data, the access to this data area can be coordinated between themselves, using the "DONE" parameter, for example. Data consistency of the communication areas transmitted locally with a communication block can thus be ensured in the user program.

S7 communication functions such as SFB 14 "GET", SFB 15 "PUT" react differently because no block is needed in the user program of the destination device. In this case the size of data consistency has to be taken into account beforehand during the programming phase.

3.3.2 Access to the Working Memory of the CPU

The communication functions of the operating system access the working memory of the CPU in fixed block lengths. The block size is a variable length up to a maximum of 462 bytes.

3.3.3 Reading from and Writing to a DP Standard Slave Consistently

Writing Data Consistently to a DP Standard Slave Using SFC 14 "DPRD_DAT"

Using SFC 14 "DPRD_DAT" (read consistent data of a DP standard slave) you can consistently read the data of a DP standard slave.

The data read is entered into the destination range defined by RECORD if no error occurs during the data transmission.

The destination range must have the same length as the one you have configured for the selected module with STEP 7.

By invoking SFC 14 you can only access the data of one module / DP ID at the configured start address.

For information on SFC 14, refer to the corresponding Online Help and to the *"System and Standard Functions"* manual

3.3.4 Writing Data Consistently to a DP Standard Slave Using SFC 15 "DPWR_DAT"

Using SFC 15 "DPWR_DAT" (write consistent data to a DP standard slave) you can consistently write data to the DP standard slave addressed in the RECORD.

The source range must have the same length as the one you have configured for the selected module with STEP 7.

Note

The Profibus DP standard defines the upper limit for the transmission of consistent user data (see following section). Typical DP standard slaves adhere to this upper limit. In older CPUs (<1999) there are restrictions in the transmission of consistent user data depending on the CPU. For these CPUs you can determine the maximum length of the data which the CPU can consistently read and write to and from the DP standard in the respective technical specifications under the index entry "DP Master – User data per DP slave". Newer CPUs are capable of exceeding the value for the amount of data that a DP standard slave can send and receive.

Upper Limit for the Transmission of Consistent User Data to a DP Slave

The Profibus DP standard defines the upper limit for the transmission of consistent user data to a DP slave. For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP slave.

During the configuration you can determine the size of the consistent area. You can set a maximum length of consistent data at 64 words = 128 bytes in the special identification format (SKF) (128 bytes for inputs and 128 bytes for outputs); the data block size cannot exceed this.

This upper limit only applies to pure user data. Diagnostics and parameter data are regrouped into full records and therefore always transferred consistently.

In the general identification format (AKF) the maximum length of consistent data can be set at 16 words = 32 bytes (32 bytes for inputs and 32 bytes for outputs); the data block size cannot exceed this.

Note in this context that a CPU 41x in a general environment acting as a DP slave on a third-party master (connection defined by GSD) has to be configured with the general identification format. The transfer memory of a CPU 41x acting as a DP slave to the PROFIBUS DP can therefore be a maximum of 16 words = 32 bytes.

For information on SFC 15, refer to the corresponding Online Help and to the *"System and Standard Functions"* manual

3.3.5 Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs describedin this manual. The data area of a DP slave that should transfer consistently is transferred to a process image partition. The information in this area is therefore always consistent. You can subsequently use load/transfer commands (such as L EW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

An I/O access error does not occur with direct access (e.g. L PEW or T PAW).

The following is important for converting from the SFC14/15 method to the process image method:

- When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- SFC 50 "RD_LGADR" outputs another address area with the SFC 14/15 method as with the process image method.
- If you are using a CP 443-5 ext the simultaneous use of SFC 14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Example:

The following example (of the process image partition 3 "TPA 3") shows such a configuration in HW Config:

- TPA 3 at output: These 50 bytes are stored consistent in the process image partition 3 (pull-down list "Consistent over -> entire length") and can therefore be read through the normal "load input xy" commands.
- Selecting "Process Image Partition -> ——" under input in the pull-down menu means: do not store in a process image. Then the handling can only be performed using the system functions SFC14/15.

	<u>J</u> nit:	Consistent over:	
50 🛨	Byte 🗾	Total length 💌	
PIP 3	•		
Length: l	Jni <u>t</u> :	Consistent over:	
20 🕂	Byte 💌	Total length 💌	
	•		
acturer:			
	PIP 3	PIP 3 Length: Unit: 20 Byte	PIP 3 Length: Unit: Consistent over: 20 Byte Total length

Memory Concept and Startup Scenarios 4

Chapter Overview

In Section	on You will find	
4.1	Overview of the Memory Concept of S7-400 CPUs	4-2
4.2	Overview of the Startup Scenarios for S7-400-CPUs	4-5

4.1 Overview of the Memory Concept of S7-400 CPUs

Organization of Memory Areas

You can divide the memory of the S7 CPUs into the following areas:

External load memory RAM with battery backup or retentive flash memory	Load memory For project data (blocks,
Integrated load memory RAM with battery backup	symbols, comments, configuration and parameter assignment data
Working memory code	
For the program	
RAM with battery backup	
Process image of inputs and output s	Wedding
Diagnostic buffer	For runtime-relevant blocks
Working memory data	
For data	
RAM with battery backup	
Local data stack	
System memory	
Contains flags, timers, counters,	
block stack and interrupt stack	
RAM with battery backup	

Important Note for CPUs with Configurable Division of the Working Memory

If you use parameter assignment to change the division of the working memory, the working memory is reorganized when the system data are downloaded to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for code or data blocks is changed if you change the following parameters for loading the system data:

- Size of the process image (byte by byte; "Cycle/Clock Memory" tab)
- Communication resources (S7-400 only; "Memory" tab)
- Size of the diagnostic buffer ("Diagnostics/Clock" tab)
- Number of local data for all priority classes ("Memory" tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory in the CPU, you must take into consideration the following memory requirements when assigning parameters:

Parameter	Required Working Memory	In Code/Data Memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of diagnostic buffer	32 bytes per entry in the diagnostic buffer	Code memory
Volume of local data	1 byte per byte of local data	Data memory

Table 4-1 Memory Requirements

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Working memory for the runtime-relevant blocks (code blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as memory markers, timers, and counters. The system memory also receives the block stack and the interrupt stack.
- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program when a block is called for its temporary data. These data are only valid as long as the block is active.

By changing the default values for the process image, local data, diagnostic buffer and communication resources (see the object properties of the CPU in HWConfig), you can control the working memory available to the runtime-relevant blocks.

Notice

Please note the following if you enlarge the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the enlarged process image. This particularly applies to IP and WF modules that you operate in the S5 adapter casing in a S7-400.

Flexible Memory Capacity

• Working memory:

The capacity of the working memory is determined by selecting the appropriate CPU from the graded range of CPUs.

• Load memory:

The integrated load memory is sufficient for small and medium-sized programs.

The load memory can be increased for larger programs by inserting the RAM memory card.

Flash memory cards are also available to ensure that programs are retained in the event of a power failure even if there isn't a backup battery. Flash memory cards can also be used (as of 4 MB) to send and execute operating system updates.

Backup

 The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

4.2 Overview of the Startup Scenarios for S7-400 CPUs

Cold Restart

• At the restart, all data (process image, memory markers, timers, counters and data blocks) are reset to the start values stored in the program (load memory), irrespective of whether they were configured as retentive or non-retentive.

Retentive flags, timers and counters retain their last valid value.

All All DBs assigned the "Non Retain" attribute are reset to the load values. The remaining blocks retain their last valid value.

• Program processing is started from the beginning again (startup OB or OB 1).

Warm Restart

• At a warm restart, the process image and the non-retentive memory markers, timers and counters are reset.

Retentive flags, timers and counters retain their last valid value.

- Program execution is started from the beginning again (startup OB or OB 1).
- When the power supply is interrupted, a warm restart is only possible in backup mode.

Hot Restart

- At a hot restart, all the data, including the process image, retain their last valid value.
- Program processing is resumed at the breakpoint.
- The outputs are not changed until the end of the current cycle.
- When the power supply is interrupted, a restart is only possible in backed-up mode.

Automation System S7-400 CPU Specifications A5E00267840-03

Cycle and Reaction Times of the S7-400

This chapter explains the composition of the cycle and reaction times of the S7-400.

You can display the cycle time of your user program on the relevant CPU using the programming device (see manual *Configuring Hardware and Communication Connections with STEP 7 Version 5.0* or higher).

Examples will illustrate how you calculate the cycle time.

The reaction time is important for monitoring a process. This chapter provides a detailed description of how to calculate this. If you use a CPU 41x-2 DP as a master in the PROFIBUS DP network, you also have to take into account DP cycle times (see Section 5.5).

Chapter Overview

Section	Description	
5.1	Cycle Time	5-2
5.2	Cycle Time Calculation	5-4
5.3	Different Cycle Times	5-7
5.4	Communication Load	5-9
5.5	Reaction Time	5-12
5.6	How Cycle and Reaction Times Are Calculated	5-17
5.6	Examples of Calculating the Cycle Time and Reaction Time	5-17
5.8	Interrupt Reaction Time	5-21
5.9	Example of Calculating the Interrupt Reaction Time	5-23
5.10	Reproducibility of Time-Delay and Watchdog Interrupts	5-24

Further Information

You will find further information on the following processing times in the S7-400 Instruction List. It lists all the *STEP 7* instructions that can be processed by the relevant CPUs, together with their execution times and all the SFCs/SFBs integrated in the CPUs and the IEC functions that can be called in *STEP 7*, together with their processing times.

5.1 Cycle Time

In this chapter you will learn about the composition of the cycle time and how you can calculate the cycle time.

Definition of the Cycle Time

The cycle time is the time which the operating system needs to process a program run - in other words, an OB 1 run - and all the program segments and system activities that interrupt that run.

This time is monitored.

Time-Sharing Model

Cyclic program scanning, and thus also processing of the user program, is performed in time slices. So that you can better appreciate these processes, we will assume in the following that each time slice is exactly 1 ms long.

Process Image

The process signals are read or written prior to program scanning so that a consistent image of the process signals is available to the CPU for the duration of cyclic program scanning. Then the CPU does not directly access the signal modules during program scanning when the address area "inputs" (I) and "outputs" (O) are addressed, but addresses instead the internal memory area of the CPU on which the image of the inputs and outputs is located.

The Cyclic Program Scanning Process

The following table and figure illustrate the phases of cyclic program scanning.

Table 5-1 Cyclic Program Scanning

Step	Process
1	The operating system starts the scan cycle monitoring time.
2	The CPU writes the values from the process-image output table in the output modules.
3	The CPU reads out the status of the inputs at the input modules and updates the process-image input table.
4	The CPU processes the user program in time slices and performs the operations specified in the program.
5	At the end of a cycle, the operating system executes pending tasks, such asthe loading and clearing of blocks.
6	The CPU then goes back to the beginning of the cycle after the configured minimum cycle time, as necessary, and starts cycle time monitoring again.

Parts of the Cycle Time

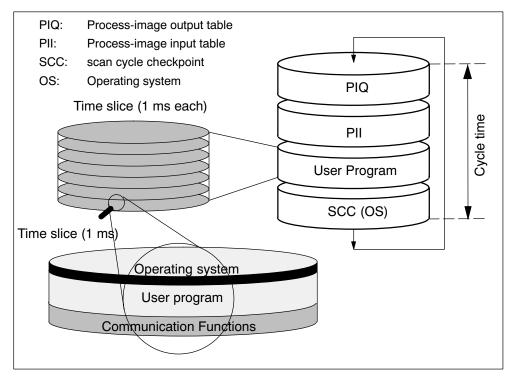


Figure 5-1 Parts and Composition of the Cycle Time

5.2 Cycle Time Calculation

Increasing the Cycle Time

Basically, you should note that the cycle time of a user program is increased by the following:

- Time-driven interrupt processing
- Hardware interrupt processing (see also Section 5.8)
- Diagnostics and error handling (see also Section 5.9)
- Communications via the MPI and CPs connected via the communication bus (for example, Ethernet, Profibus, DP); contained in the communication load
- Special functions such as control and monitoring of variables or block status
- Transfer and clearance of blocks, compression of the user program memory

Factors that Influence the Cycle Time

The following table indicates the factors that influence the cycle time.

Factors	Remark	
Transfer time for the process-image output table (PIQ) and the process-image input table (PII)	see Table 5-3	
User program processing time	is calculated from the execution times of the different instructions (see <i>S7-400 Instruction List</i>).	
Operating system scan time at scan cycle checkpoint	see Table 5-4	
Increase in the cycle time from communications	You set the maximum permissible cycle load expected for communication in % in <i>STEP 7</i> (manual <i>Programming with STEP 7</i>). See Section 5.4.	
Impact of interrupts on the cycle time	Interrupt can interrupt the user program at any time. see Table 5-5	

Table 5-2 Factors that Influence the Cycle Time

Note

With CPUs produced prior to October 1998, updating of the process image of the outputs takes place before the scan cycle checkpoint.

Process Image Updating

The table below shows the CPU times for process image updating (process image transfer time). The times listed in the table are "ideal values" that may be increased by the occurrence of interrupts and by CPU communications.

The transfer time for process image updating is calculated as follows

С	+ portion in central rack (from line A of the following table)
	 + portion in expansion rack with local connection (from line B)
	+ portion in expansion rack with remote connection (from line C)
	+ portion via integrated DP interface (from line D)
	+ portion of consistent data via integrated DP interface (from line E1)
	+ portion of consistent data via external DP interface (from line E2)
	= transfer time for process image updating

The following tables list the individual portions of the transfer times for updating the process image (process image transfer time), once for standard CPUs and once for redundant CPUs. The times listed in the table are "ideal values" that may be increased by the occurrence of interrupts and by CPU communications.

Table 5-3 Portions of the process image transfer time

	Portions n = number of bytes in the process image c= number of consistency areas ****) in the process image	CPU 412	CPU 414	CPU 416	CPU 417
Κ	Base load	22 µs	18 µs	10 µs	7 μs
А	In the central rackI *)	n * 1,9 μs	n * 1,9 μs	n * 1,9 μs	n * 1,9 μs
В	In the expansion rack with local connection $^{*)}$	n * 5 μs	n * 5 μs	n * 5 μs	n * 5 μs
С	In the expansion rack with remote connection *) **) Read	n * 12 μs	n * 12 μs	n * 12 μs	n * 12 μs
	Write	n * 11 μs	n * 11 μs	n * 11 μs	n * 11 μs
D	In the DP area for the integrated DP interface	13 μs + n * 0,4 μs	4,0 μs + n * 0,25 μs	2,0 μs + n * 0,1 μs	1,5 μs + n * 0,1 μs
E	In the DP area for the external DP interface (CP 443-5 extended)	2,3 μs + n * 2,3 μs	1,3 μs + n * 2,0 μs	1,0 μs + n * 2,0 μs	1,0 μs + n * 2,0 μs
F 1	Consistent data in the process image for the integrated DP interface	k * 45 μs + n*0,25 μs	k * 4,0 μs + n*0,25 μs	k * 2,0 μs + n*0,15 μs	k * 1,5 μs + n*0,21 μs
F 2	Consistent data in the process image for the external DP interface (CP 443-5 extended)	k * 33 μs + n *2,0 μs	k * 2,1 μs + n *0,5 μs	k * 2,0 μs +n * 0,5 μs	k * 2,0 μs + n *1,9 μs

*) In the case of I/O modules that are plugged into the central rack or an expansion rack, the specified value contains the runtime of the I/O module

**) Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

***)The areas set in HW Config that are written to or read from the I/O at once and are therefore consistent.

Operating System Scan Time at the Scan Cycle Checkpoint

The table below lists the operating system scan times at the scan cycle checkpoint of the CPUs.

Table 5-4 Operating system scan time at scan cycle checkpoint

Process	CPU 412-1	CPU 412-2	CPU 414-2	CPU 414-3	CPU 416-2	CPU 416-3	CPU 417-4
Scan cycle	331 μs to	381 μs to	222 μs to	270 μs to	140 μs to	179 μs to	164 μs to
control at	545 μs	560 μs	348 μs	391 μs	220 μs	260 μs	233 μs
the SCC	Ø 339 μs	Ø 391 μs	Ø 228 μs	Ø 276 μs	Ø 144 μs	Ø 184 μs	Ø 168 μs

Increase in Cycle Time by Nesting Interrupts

CPU	Hardware Interrupt	Diagnostic Interrupt	Day Interrupt	Time-Delay Interrupt	Watchdog Interrupt	Programming/ Periphery Access Error
CPU 412-1/-2	696 µs	752 μs	584 μs	504 μs	504 μs	224 μs / 232 μs
CPU 414-2/-3	420 μs	450 μs	350 µs	300 µs	300 µs	135 μs / 140 μs
CPU 416-2/-3	280 µs	305 µs	230 µs	200 μs	200 μs	90 µs / 90 µs
CPU 417-4	260 µs	280 µs	210 μs	185 μs	185 µs	80 μs / 90 μs

 Table 5-5
 Increase in Cycle Time by Nesting Interrupts

You have to add the program execution time at the interrupt level to this increase.

If several interrupts are nested, their times must be added together.

5.3 Different Cycle Times

The length of the cycle time (T_{cyc}) is not identical in each cycle. The following figure shows different cycle times, T_{cyc1} and T_{cyc2} . T_{cyc2} is longer than T_{cyc1} , because the cyclically scanned OB 1 is interrupted by a time-of-day interrupt OB (in this instance, OB 10).

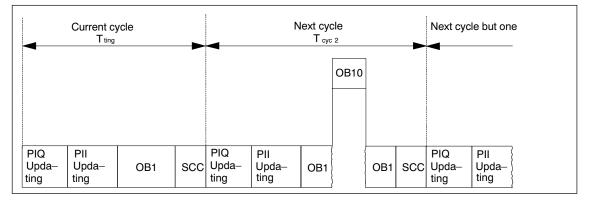


Figure 5-2 Different Cycle Times

A further reason for cycle times of different length is the fact that the execution time of blocks (for example, OB 1) can vary on account of:

- Conditional instructions
- Conditional block calls
- Different program paths
- Loops, etc.

Maximum Cycle Time

You can modify the default maximum cycle time in STEP 7 (cycle monitoring time). If this time has expired, OB 80 is called, and in it you can define how you want the CPU to respond to the time error. If you do not retrigger the cycle time with SFC 43, OB 80 doubles the cycle time at the first call. In this case, the CPU goes to STOP at the second call of OB 80.

If there is no OB 80 in the CPU memory, the CPU goes to STOP.

Minimum Cycle Time

You can set a minimum cycle time for a CPU in STEP 7. This is practical if

- you want the intervals of time between the start of program scanning of OB1 (free cycle) to be roughly of the same length, or
- updating of the process images would be performed unnecessarily often with too short a cycle time, or
- you want to process a program with the OB 90 in the background (not CPU 41x-4H).

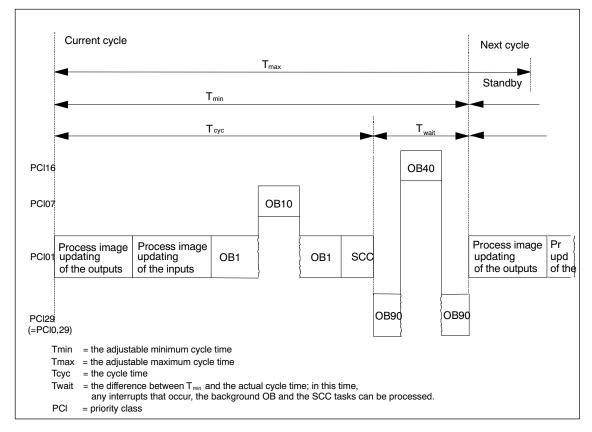


Figure 5-3 Minimum Cycle Time

The actual cycle time is the sum of T_{cyc} and T_{wait} . It is always greater than or equal to T_{min} .

5.4 Communication Load

The CPU operating system continually makes available to communications the percentage you configured for the overall CPU processing performance (time sharing). If this processing performance is not required for communications, it remains available for other processing tasks.

In the hardware configuration, you can set the load due to communications between 5% and 50%. By default, the value is set to 20%.

This percentage should be regarded as an average value, in other words, the communications component can be considerably greater than 20% in a time slice. On the other hand, the communications component in the next time slice is only a few or zero percent. This fact is also expressed by the following formula:

Actual cycle time	= cycle time	100 100 - "configured communication load in %"		
Round up the result to the next whole number !				

Figure 5-4 Formula: Influence of Communication Load

Data consistency

The user program is interrupted for communications processing. The interrupt can be executed after any instruction. These communication jobs can modify the program data.

This means that the data consistency cannot be guaranteed for the duration of several accesses.

The manner in which you can guarantee consistency enduring for more than just one instruction is explained in the manual *System Software for S7-300/400 System and Standard Functions*, in the chapter on *Overview of S7 Communications and S7 Basic Communications*.

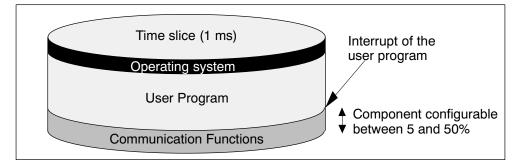


Figure 5-5 Breakdown of a Time Slice

Of the part remaining, the operating system of the S7-400 requires only a negligibly small amount for internal tasks.

Example: 20 % Communication Load

You have configured a communication load of 20% in the hardware configuration.

The calculated cycle time is 10 ms.

A 20% communication load means that, on average, 200 μ s and 800 μ s of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 800 μ s = 13 time slices to process one cycle. This means that the actual cycle time is 13 times a 1 ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

This means that 20% communications do not increase the cycle linearly by 2 ms but by 3 ms.

Example: 50 % Communication Load

You have configured a communication load of 50% in the hardware configuration.

The calculated cycle time is 10 ms.

This means that 500 μ s of each time slice remain for the cycle. The CPU therefore requires 10 ms / 500 μ s = 20 time slices to process one cycle. This means that the actual cycle time is 20 ms if the CPU fully utilizes the configured communication load.

A 50 % communication load means that, on average, 500 μ s and 500 μ s of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 500 μ s = 20 time slices to process one cycle. This means that the actual cycle time is 20 times a 1 ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communications do not increase the cycle linearly by 5 ms but by 10 ms.

Dependency of the Actual Cycle Time on the Communication Load

The following figure describes the non-linear dependency of the actual cycle time on the communication load. As an example, we have chosen a cycle time of 10 ms.

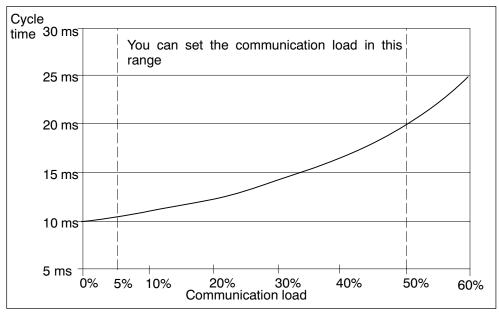


Figure 5-6 Dependency of the Cycle Time on the Communication Load

Further Effect on the Actual Cycle Time

Due to the increase in the cycle time as a result of the communications component, even more asynchronous events occur, from a statistical point of view, within an OB 1 cycle than, say, interrupts. This also increases the OB 1 cycle. This increase depends on how many events occur per OB 1 cycle and how long event processing lasts.

Notes

- Check the effects of a change of the value for the parameter "Cycle load due to communications" in system operation.
- The communication load must be taken into account when you set the maximum cycle time, since time errors will occur if it is not.

Recommendations

- If possible, apply the default value.
- Use a larger value only if the CPU is being used primarily for communication purposes and the user program is non-time-critical. In all other cases select a smaller value.

5.5 Reaction Time

Definition of the Reaction Time

The reaction time is the time from an input signal being detected to changing an output signal linked to it.

Variation

The actual reaction time is somewhere between a shortest and a longest reaction time. For configuring your system, you must always reckon with the longest reaction time.

The shortest and longest reaction times are analyzed below so that you can gain an impression of the variation of the reaction time.

Factors

The reaction time depends on the cycle time and on the following factors:

- Delay in the inputs and outputs
- Additional DP cycle times on the PROFIBUS-DP network
- Execution of the user program

Delay in the Inputs and Outputs

Depending on the module, you must heed the following time delays:

- For digital inputs: the input delay
- For interrupt-capable digital inputs: the input delay +
 the module-internal preparation time
- For digital outputs: negligible time delays
- For relay outputs: typical time delays from 10 to 20 ms. The delay of the relay outputs depends, among other things, on the temperature and voltage.
- For analog inputs: cycle time of analog input module
- For analog outputs: response time of the analog output module

The time delays can be found in the technical specifications of the signal modules.

DP Cycle Times on the PROFIBUS-DP Network

If you have configured your PROFIBUS-DP network with *STEP 7*, then *STEP 7* will calculate the typical DP cycle time that must be expected. You can then have the DP cycle time of your configuration displayed for the bus parameters on the programming device.

The following figure will provide you with an overview of the DP cycle time. We assume in this example that each DP slave has 4 byte of data on average.

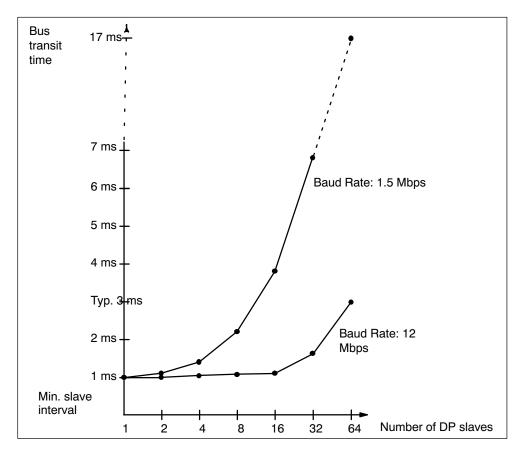
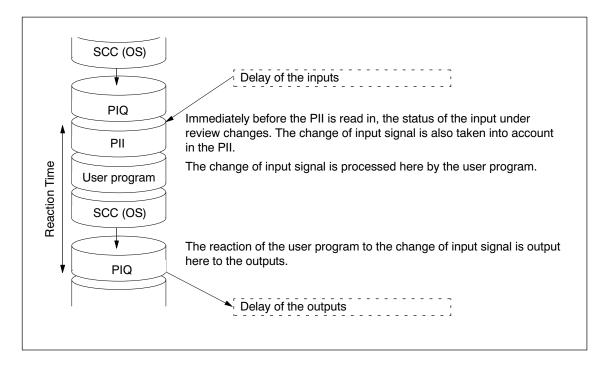


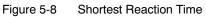
Figure 5-7 DP Cycle Times on the PROFIBUS-DP Network

If you are operating a PROFIBUS-DP network with more than one master, you must take the DP cycle time into account for each master. In other words, perform a separate calculation for each master and add the results together.

Shortest Reaction Time

The following figure illustrates the conditions under which the shortest reaction time is achieved.





Calculation

The (shortest) reaction time is made up as follows:

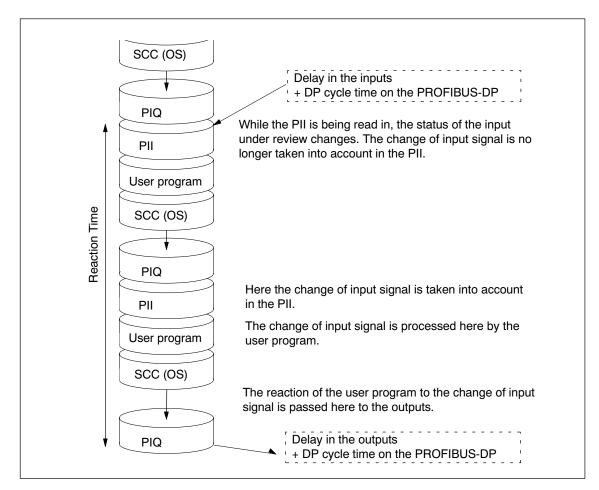
- 1 × process image transfer time of the inputs +
- 1 × process image transfer time of the outputs +
- 1 × program processing time +
- 1 × operating system processing time at SCC +
- · Delay in the inputs and outputs

This is equivalent to the sum of the cycle time and the delay in the inputs and outputs.

Note

If the CPU and signal module are not in the central rack, you have to add double the runtime of the DP slave frame (including processing in the DP master).

Longest Reaction Time



The following figure shows you how the longest reaction time results.

Figure 5-9 Longest Reaction Time

Calculation

The (longest) reaction time is made up as follows:

- 2 × process image transfer time of the inputs +
- 2 × process image transfer time of the outputs +
- 2 × operating system processing time +
- 2 × program processing time +
- 2 × runtime of the DP slave frame (including processing in the DP master) +
- Delay in the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.

I/O Direct Accesses

You can achieve faster reaction times by direct access to the I/O in the user program, for example with

- L PIB or
- T PQW

you can avoid the reaction times in part, as described above.

Reducing the Reaction Time

In this way the maximum reaction time is reduced to

- Delay in the inputs and outputs
- Runtime of the user program (can be interrupted by high-priority interrupt handling)
- Runtime of direct accesses
- Twice the bus transit time of DP

The following table lists the execution times of direct accesses by the CPU to I/O modules. The times shown are "ideal values".

Table 5-6 Reducing the Reaction Time

Type of Access	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4	
I/O Module					
Read byte	3.0 μs	2.7 μs	2.4 μs	2.3 μs	
Read word	4.7 μs	4.4 μs	3.9 µs	3.8 µs	
Read double word	7.6 μs	7.2 μs	6.9 μs	6.7 μs	
Write byte	3.2 μs	2.8 μs	2.4 μs	2.3 μs	
Write word	4.7 μs	4.5 μs	4.1 μs	4.0 μs	
Write double word	8.1 μs	7.7 μs	7.3 μs	7.2 μs	
Expansion device with close coupling					
Read byte	6.4 μs	6.2 μs	5.8 μs	5.7 μs	
Read word	11.8 μs	11.3 μs	10.9 μs	10.8 μs	
Read double word	21.7 μs	21.3 µs	20.9 µs	20.8 µs	
Write byte	7.9 μs	5.8 µs	5.6 µs	5.5 μs	
Write word	11.2 μs	11.0 μs	10.6 μs	10.5 μs	
Write double word	21.1 μs	20.7 μs	20.4 μs	20.2 μs	

Type of Access	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4	
Reading bytes in the expansion device with remote coupling					
Read byte	11.4 μs	11.4 μs	11.3 μs	11.3 μs	
Read word	22.9 µs	22.9 µs	22.8 µs	22.8 µs	
Read double word	45.9 μs	45.9 μs	45.9 μs	45.9 μs	
Write byte	11.0 μs	10.9 μs	10.8 µs	10.8 μs	
Write word	22.0 µs	22.0 µs	21.9 µs	21.9 µs	
Write double word	44.0 μs	44.0 μs	44.0 μs	44.0 μs	

The specified times are merely CPU processing times and apply, unless otherwise stated, to signal modules in the central rack.

Note

You can similarly achieve fast reaction times by using hardware interrupts; refer to Section 5.8.

5.6 How Cycle and Reaction Times Are Calculated

Cycle time

- 1. Using the Instruction List, determine the runtime of the user program.
- 2. Calculate and add the transfer time for the process image. You will find guide values for this in Table 5-3.
- 3. Add to it the processing time at the scan cycle checkpoint. You will find guide values for this in Table 5-4.

The result you achieve is the cycle time.

Increasing the Cycle Time with Communication and Interrupts

4. Multiply the result by the following factor:

100

100 - "configured communication load in %"

 Using the Instruction List, calculate the runtime of the program sections that hardware interrupts. Add to it the relevant value in Table 5-5. Multiply this value by the factor from step 4. Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result you obtain is approximately the actual cycle time. Make a note of the result.

Shortest Reaction Time	Longest Reaction Time		
6. Then, calculate the delays in the inputs and outputs and, if applicable,	6. Multiply the actual cycle time by a factor of 2.		
the DP cycle times on the PROFIBUS DP network.	7. Then, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.		
7. The result you obtain is the shortest reaction time.	8. The result you obtain is the longest reaction time.		

Table 5-7 Example of Calculating the Reaction Time

5.7 Examples of Calculating the Cycle Time and Reaction Time

Example I

You have installed an S7-400 with the following modules in the central rack:

- One CPU 414-2
- Two digital input modules SM 421; DI 32 x DC 24 V (4 byte each in PA)
- Two digital output modules SM 422; DO 32 x DC 24 V/0.5A (4 byte each in PA)

User Program

According to the Instruction List, your user program has a runtime of 15 ms.

Cycle Time Calculation

The cycle time for the example results from the following times:

• Process image transfer time

Process image: $13 \mu s + 16$ byte x $1.5 \mu s = approx$. **0.037 ms**

 Operating system runtime at scan cycle checkpoint: approx. 0.23 ms

The cycle time for the example results from the sum of the times listed:

Cycle time = 12.0 ms + 0.037 ms + 0.23 ms = 12.27 ms.

Calculation of the Actual Cycle Time

- Allowance of the communication load (default value: 20%): 12.27 ms * 100 / (100-20) = 15.24 ms.
- There is no interrupt handling.

The rounded actual cycle time is thus 15.3 ms.

Calculation of the Longest Reaction Time

- Longest reaction time
 15.3 ms * 2 = 30.6 ms.
- The delay in the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt handling.

Rounded off, the longest reaction time is thus = 31 ms.

Example II

You have installed an S7-400 with the following modules:

- One CPU 414-2
- Four digital input modules SM 421; DI 32 x DC 24 V (4 byte each in PA)
- Three digital output modules SM 422; DO 16 x DC 24 V/2A (2 byte each in PA)
- Two analog input modules SM 431; AI 8 x 13 bit (not in PA)
- Two analog output modules SM 432; AO 8 x 13 bit (not in PA)

CPU Parameters

The CPU has been assigned parameters as follows:

• Cycle load due to communications: 40%

User Program

According to the Instruction List, the user program has a runtime of 10.0 ms.

Cycle Time Calculation

The theoretical cycle time for the example results from the following times:

- Process image transfer time
 - Process image: $13 \ \mu s + 22$ byte x 1.5 $\ \mu s = approx$. **0.049 ms**
- Operating system runtime at scan cycle checkpoint: approx. 0.23 ms

The cycle time for the example results from the sum of the times listed:

Cycle time = 10.0 ms + 0.049 ms + 0.23 ms = 10.28 ms.

Calculation of the Actual Cycle Time

- Allowance of communication load: 10.28 ms * 100 / (100-40) = 37 ms.
- A time-of-day interrupt having a runtime of 0.5 ms is triggered every 100 ms. The interrupt cannot be triggered more than once during a cycle: 0.5 ms + 0.35 ms (in Table 5-5) = 0.85 ms. Allowance for communication load: 0.85 ms * 100 / (100-40) = 1.42 ms.
- 17.1 ms + 1.42 ms = **18.52 ms**.

The actual cycle time is therefore 18.5 ms taking into account the time slices.

Calculation of the Longest Reaction Time

- Longest reaction time 8.5 ms * 2 = 37 ms.
- Delays in the inputs and outputs
 - The digital input module SM 421; DI 32 x DC 24 V has an input delay of not more than 4,8 ms per channel
 - The digital output module SM 422; DO 16 x DC 24 V/2A has a negligible output delay.
 - The analog input module SM 431; AI 8 x 13 bit was assigned parameters for 50 Hz interference frequency suppression. This results in a conversion time of 25 ms per channel. Since 8 channels are active, a cycle time of **200 ms** results for the analog input module.
 - Analog output module SM 432; AO 8 x 13 bit was assigned parameters for the measuring range from 0 to 10V. This results in a conversion time of 0.3 ms per channel. Since 8 channels are active, a cycle time of 2.4 ms results. To this must be added the settling time for the resistive load, which is 0.1 ms. A response time of 2.5 ms therefore results for an analog output.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- **Case 1:** When a digital signal is read in, an output channel of the digital output module is set. This produces a reaction time of:

Reaction time= 37 ms + 4.8 ms = 41.8 ms.

• **Case 2:** An analog value is read in and an analog value output. This produces a reaction time of:

Reaction time = 37 ms + 200 ms + 2.5 ms = 239.5 ms.

5.8 Interrupt Reaction Time

Definition of the Interrupt Reaction Time

The interrupt reaction time is the time from when an interrupt signal first occurs to calling the first instruction in the interrupt OB.

The following general rule applies: Interrupts having a higher priority take precedence. This means that the interrupt reaction time is increased by the program processing time of the higher priority interrupt OBs and interrupt OBs with the same priority that have not yet been processed (queue).

Note

The interrupt reaction times can be delayed by read and write jobs with a high data volume (approx. 460 byte).

When interrupts are transferred between a CPU and DP master, only a diagnostic **or** hardware interrupt can be currently reported at any time from a DP line.

Calculation

	Min. interrupt reaction time of the CPU		Max. interrupt reaction time of the CPU
+	min. interrupt reaction time of the	+	max. interrupt reaction time of the
	signal modules		signal modules
+	DP cycle time on PROFIBUS-DP	+	2 * DP cycle time on PROFIBUS-DP
=	Shortest Reaction Time	=	Longest Reaction Time

Figure 5-10 Calculating the Interrupt Reaction Time

Hardware Interrupt and Diagnostic Interrupt Reaction Times of CPUs

Table 5-8Hardware Interrupt and Diagnostic Interrupt Reaction Times; Maximum Interrupt
Reaction Time Without Communication

CPU	read	interrupt tion nes	Diagnostic interrupt reaction times		Asynchronous error (OB 85, at process image update)
	min.	max.	min.	max.	
412-1/-2	544 μs	560 μs	608 μs	624 μs	392 µs
414-2/-3	325 μs	335 µs	365 μs	375 μs	300 µs
416-2/-3	220 μs	230 µs	245 μs	255 μs	200 μs
417-4	200 µs	210 μs	225 μs	235 µs	180 μs

Increasing the Maximum Interrupt Reaction Time with Communication

The maximum interrupt reaction time increases when communication functions are active. The increase is calculated with the following formula:

CPU 412: $tv = 200 \ \mu s + 1000 \ \mu s \ x \ n\%$ CPU 414-417: $tv = 100 \ \mu s + 1000 \ \mu s \ x \ n\%$ where n = cycle load from communication

Signal Modules

The hardware interrupt reaction time of the signal modules is made up as follows:

• Digital input modules

Hardware interrupt reaction time = internal interrupt processing time + input delay

You will find the times in the data sheet of the digital input module concerned.

• Analog input modules

Hardware interrupt reaction time = internal interrupt processing time + conversion time

The internal interrupt processing time of the analog input modules is negligible. The conversion times can be taken from the data sheet of the analog input module concerned.

The diagnostic interrupt reaction time of the signal modules is the time which elapses between a diagnostics event being detected by the signal module and the diagnostic interrupt being triggered by the signal module. This time is so small that it can be ignored.

Hardware Interrupt Processing

When the hardware interrupt OB 40 is called, the hardware interrupt is processed. Interrupts with higher priority interrupt hardware interrupt processing, and direct access to the I/O is made when the instruction is executed. When hardware interrupt processing is completed, either cyclic program processing is continued or other interrupt OBs with the same or a lower priority are called and processed.

5.9 Example of Calculating the Interrupt Reaction Time

Parts of the Interrupt Reaction Time

As a reminder, the hardware interrupt reaction time is made up of the following:

- Hardware interrupt reaction time of the CPU
- Hardware interrupt reaction time of the signal module.
- $2 \times DP$ cycle time on the PROFIBUS-DP

Example: You have an S7-400 consisting of a CPU 416-2 and 4 digital modules in the central rack. One digital input module is the SM 421; DI 16×UC 24/60 V; with hardware and diagnostic interrupts. In the parameter assignment of the CPU and the SM, you have only enabled the hardware interrupt. You do not require time-driven processing, diagnostics and error handling. You have assigned an input delay of 0.5 ms for the digital input module. No activities at the scan cycle checkpoint are required. You have set a cycle load from communication of 20%.

Calculation

The hardware interrupt reaction time for the example results from the following times:

- Hardware interrupt reaction time of the CPU 416-2: approx. 0.35 ms
- Increase from communication in accordance with the formula shown in Table 5-8 :

 $100 \ \mu s + 1000 \ \mu s \times 20\% = 300 \ \mu s = 0.3 \ ms$

- Hardware interrupt reaction time of the SM 421; DI 16 x UC 24/60 V:
 - Internal interrupt processing time: 0.5 ms
 - Input delay: 0.5 ms
- Since the signal modules are plugged into the central rack, the DP cycle time on the PROFIBUS-DP is not relevant.

The hardware interrupt reaction time results from the sum of the listed times:

Hardware interrupt reaction time = 0.23 ms + 0.3 ms + 0.5 ms + 0.5 ms = approx.**1.53 ms**.

This calculated hardware interrupt reaction time is the time from a signal being applied across the digital input to the first instruction in OB 40.

5.10 Reproducibility of Time-Delay and Watchdog Interrupts

Definition of "Reproducibility"

Time-delay interrupt:

The deviation with time from the first instruction of the interrupt OB being called to the programmed interrupt time.

Watchdog interrupt

The variation in the time interval between two successive calls, measures between the first instruction of the interrupt OB in each case.

Reproducibility

Table 5-9 contains the reproducibility of time-delay and watchdog interrupts of the CPUs.

Module	Reproducibility				
	Time-Delay Interrupt:	Watchdog Interrupt			
CPU 412-1/-2	–220 μs / +220 μs	–35 μs / +35 μs			
CPU 414-2/-3	–235 μs / +205 μs	–35 μs / +35 μs			
CPU 416-2/-3	–210 μs / +210 μs	–20 μs / +20 μs			
CPU 417-4	–220 μs / +200 μs	–20 μs / +20 μs			

Table 5-9Reproducibility of Time-Delay and Watchdog Interrupts of the
CPUs.

These times apply only if the interrupt can be executed at this time and not, for example, delayed by interrupts with higher priority or interrupts of identical priority that have not yet been executed.

6

Technical Specifications

Chapter overview

In Section	You Will Find	On Page
6.1	Technical Specifications of the CPU 412-1; (6ES7412-1XF04-0AB0)	6-2
6.2	Technical Specifications of the CPU 412-2; (6ES7412-2XG04-0AB0)	6-6
6.3	Technical Specifications of the CPU 414-2; (6ES7414-2XG04-0AB0)	6-10
6.4	Technical Specifications of the CPU 414-3; (6ES7414-3XJ04-0AB0)	6-14
6.5	Technical Specifications of the CPU 416-2; (6ES7416-2XK04-0AB0, 6ES7416-2FK04-0AB0)	6-18
6.6	Technical Specifications of the CPU 416-3; (6ES7416-3XL04-0AB0)	6-22
6.7	Technical Specifications of the CPU 417-4; (6ES7417-4XL04-0AB0)	6-26
6.8	Technical Specifications of the Memory Cards	6-30

6.1 Technical Specifications of the CPU 412-1; (6ES7412-1XF04-0AB0)

CPU and Firmv	vare Version	Data Areas and Their Retentivity		
MLFB Firmware version Associated programming	6ES7412-1XF04-0AB0 4.0.0 As of STEP 7 5.2 SP1	Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)	
package HF3 with HW update		Memory markers	4 Kbytes	
Memo	ory	Retentivity can be set	From MB 0 to MB 4095	
Working memory	-	 Preset retentivity 	From MB 0 to MB 15	
Integrated	72 Kbytes for code	Clock memories	8 (1 memory byte)	
C C	72 Kbytes for data	Data blocks	Max. 511 (DB 0 reserved)	
Load memory	-	• Size	Max. 64 Kbytes	
Integrated	256 Kbytes RAM	Local data (can be set)	Max. 8 Kbytes	
Expandable FEPROM	With memory card	Preset	4 Kbytes	
	(FLASH) up to 64 Mbytes	Blo	cks	
Expandable RAM	With memory card (RAM)	OBs	See instruction list	
	up to 64 Mbytes	• Size	Limited by working	
Backup with battery	Yes, all data		memory	
Processing Times		Nesting depth		
Processing times for		 Per priority class 	24	
Bit operations	0.1 μs	 Additionally in an error 	2	
 Word instructions 	0.1 μs	OB	May 050	
 Integer math instructions 	0.1 μs	FBs	Max. 256	
 Floating-point math instructions 	0.3 μs	• Size	Limited by working memory	
Timers/Counters and	Their Retentivity	FCs	Max. 256	
S7 countersRetentivity can be set	2048 From Z 0 to Z 2047	• Size	Limited by working memory	
 Preset 	From Z 0 to Z 7	Address Areas (Inputs/Outputs)	
Counting range	1 to 999	Total I/O address area	4 Kbytes/4 Kbytes	
IEC counter	Yes	Of which distributed		
Type	SFB	MPI/DP interface	2 Kbytes/2 Kbytes	
S7 timers	2048	Process Image	4 Kbytes/4 Kbytes (can be set)	
 Retentivity can be set 	From T 0 to T 2047	Preset	128 bytes/128 bytes	
Preset	No retentive timers	 Number of partial 	Max. 15	
Time range	10 ms to 9990 s	process images		
IEC timers	Yes	Consistent data	Max. 244 bytes	
• Туре	SFB	Digital channels	Max. 32768/Max. 32768	
		Of which central	Max. 32768/Max. 32768	
		Analog channels	Max. 2048/Max. 2048	
		Of which central	Max. 2048/Max. 2048	

Configu	S7 Message Functions			
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	Number of static log on for messa functions (e.g. V SIMATIC OP)	ige	Max. 8
Number of plug-in IMs	Max. 6	Symbol-related	nessages	Yes
(overall)		 Number of n 	nessages	
• IM 460	Max. 6	 Overall 		Max. 512
 IM 463-2 	Max. 4	- 100 ms	grid	None
Number of DP masters		- 500 ms	grid	Max. 256
 Integrated 	1	– 1000 ms	s arid	Max. 256
 Via IM 467 	Max. 4	 Number of a 	0	1
• Via CP 443-5 Extended	Max. 10	values per n		
IM 467 cannot be used with the	e CP 443-5 EX40	- With 10) ms grid	None
IM 467 cannot be used with the mode	e CP 443-1 EX40 in PN IO	– With 500 grid	0, 1000 ms	1
Number of plug-in S5	Max. 6	Block-related me	essages	Yes
modules via adapter casing (in the central rack) Operable function modules and communication		 Simultaneou ALARM_S/S and ALARM blocks 	Q blocks	Max. 70
processors		ALARM 8 block	s	Yes
• FM	Limited by the number of slots and the number of connections	 Number of communicat ALARM_8 b 	ion jobs for	Max. 300
• CP 440	Limited by the number of slots	blocks for S communicat	7	
• CP 441	Limited by the number of connections	set) ● Preset		150
• PROFIBUS and Ethernet	Max. 14	Process control	renorts	Yes
CPs incl. CP 443-5 Extended and IM 467		Number of archi	ves that	4
Tim	e	can log on simultaneously (SFB 37 AR SEND)		
Clock	Yes	Test a	nd Commis	sioning Functions
Buffered	Yes	Monitor/modify v		Yes
 Resolution Accuracy at Power off 	1 ms Deviation per day 1.7 s	Variables		Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
 Power on 	Deviation per day 8.6 s	A Niverski svi f	- vielela -	counters
Runtime meter	8	 Number of v 	anables	Max. 70
Number	0 to 7	Force		Yes
Value RangeGranularity	0 to 32767 hours 1 hour	 Variables 		Inputs/outputs, memory markers, distributed
Retentive	Yes			inputs/outputs
Time synchronization	Yes	Number of v	ariables	Max. 64
In PLC, on MPI and DP	as master or slave	Status block		Yes
	as master of slave	Single sequence		Yes
		Diagnostic buffe		Yes
		Number of e	entries	Max. 200 (can be set)
		Preset		120

Number of breakpoints

4

Communicati	ion Functions		1st Interface D	P Master Mode
Programming device/OP	Yes	•	Utilities	
communication Number of connectable OPs	15 without message processing, 8 with message		 Programming device/OP communication 	Yes
Number of connection	processing 16, with each of them		 Routing 	Yes
resources for S7 connections via all interfaces and CPs	reserved for PG and OPrespectively		 S7 basic communication 	Yes
Global data communication	Yes		 S7 communication 	Yes
Number of GD circuits	Max. 8		 Constant bus cycle time 	Yes
 Number of GD packages 			- SYNC/FREEZE	Yes
– Sender	Max. 8		 Enable/disable DP 	Yes
– Receiver	Max. 16		slaves	
 Size of GD packages 	Max. 64 bytes	•	Transmission rates	Up to 12 Mbps
 Of which consistent 	1 variable	•	Number of DP slaves	Max. 32
S7 basic communication	Yes	•	Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT	•	User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with
 DP Master Mode 	via SFC I_GET and I_PUT			max. 128 bytes
 User data per job 	Max. 76 bytes		Note:	
 Of which consistent 	1 variable	•	The accumulated	
S7 communication	Yes		number of input bytes at the slots may not	
 User data per job 	Max. 64 Kbytes		exceed 244	
 Of which consistent 	1 variable (462 bytes)	•	The accumulated	
S5-compatible	via FC AG_SEND and		number of output bytes	
communication	AG_RECV, max. via 10 CP 443-1 or 443-5)		at the slots may not exceed 244	
 User data per job 	Max. 8 Kbytes	•	The maximum address area of the interface	
 Of which consistent 	240 bytes		(max. 2KB inputs /2 KB	
Standard communication (FMS)	Yes (via CP and loadable FB)		outputs) accumulated by 32 slaves may not	
Inter	faces		be exceeded	
	erface	İ		DP Slave Mode
Type of interface	Integrated	•	Utilities	
Physical	RS 485/Profibus		 Monitor/modify 	Yes
Isolated	Yes		 Programming 	Yes
Power supply to interface	Max. 150 mA		 Routing 	Yes
(15 VDC to 30 VDC) Number of connection	MPI: 16	•	DDB (GSD) file	http://www.ad.siemens.de/o si_e/gsd
resources	DP: 16	•	Transmission rate	Up to 12 Mbps
MPI	onality Yes	•	Intermediate memory	244 bytes inputs/ 244 bytes outputs
PROFIBUS DP	DP master/DP slave		 virtual slots 	Max. 32
	e MPI Mode		 User data per address area 	Max. 32 bytes
 Otilities Programming 	Voc		 Of which consistent 	32 bytes
 Programming device/OP communication 	Yes			
 Routing 	Yes			
 Global data communication 	Yes			
 S7 basic communication 	Yes			
 S7 communication 	Yes			

Transmission rates
 Up to 12 Mbps

Progra	amming	Dimensions		
Programming language	LAD, FBD, STL, SCL	Mounting dimensions	25×290×219	
Instruction set	See instruction list	W×H×D (mm)		
Bracket levels	8	Slots required	1	
System functions (SFC)	See instruction list	Weight	approx. 0.72 kg	
Number of SFCs active at		Voltages	, Currents	
the same time for every		Current consumption from	Тур. 0.6 А	
strand		S7-400 bus (5 VDC)	Max. 0.7 A	
DPSYC_FR	2	Current consumption from	Total current consumption	
D_ACT_DP	4	the S7-400 bus (24 VDC) The CPU does not	of the components connected to the MPI/DP	
RD_REC	8	consume any current at	interfaces, with a maximum	
WR_REC	8	24 V, and it only makes this	of 150 mA per interface	
WR_PARM	8	voltage available at the MPI/DP interface.		
PARM_MOD	1		Ture 050 ··· A	
WR_DPARM	2	Backup current	Typ. 350 μA	
DPNRM_DG DP0Y00T	8	l and the stars the stars the s	Max. 890 μA	
RDSYSST	1 to 8	maximum backup time	See manual <i>Module</i> Specifications, chapter 3.3	
DP_TOPOL	1 See instruction list	Incoming supply of external	5 VDC to 15 VDC	
System function blocks (SFB)	See instruction list	backup voltage to the CPU		
Number of SFBs active at the same time		Power loss	Typ. 3.0 W	
 RD_REC 	8			
 WR_REC 	8			
User program protection	Password protection			
Access to consistent data in the process image	Yes			
Clock sy	nchronism			
User data per clock synchronous slave	Max. 244 bytes			
Maximum number of bytes	The following applies:			
and slaves in a process image partition	Number of bytes/100 + number of slaves <16			
Constant bus cycle time	Yes			
Shortest clock pulse	1.5 ms			
	0.5 ms without use of SFC 126, 127			
see the manual <i>Clock Synchronism</i>				
CiR synchro	onization time			
Base load	100 ns			
Time per I/O byte	200 μs			

6.2 Technical Specifications of the CPU 412-2; (6ES7412-2XG04-0AB0)

CPU an	nd Version	Data Areas and Their Retentivity		
MLFB	6ES7412-2XG04-0AB0	Total retentive data areas (including memory bits;	Total working and load memory (with backup	
Firmware version	V 4.0.0	times; counts)	battery)	
Associated programming	As of STEP 7 5.2 SP1 HF3	Flags	4 Kbytes	
package	with HW-Update	 Retentivity can be set 	From MB 0 to MB 4095	
	emory	 Preset retentivity 	From MB 0 to MB 15	
Working memory		Clock memories	8 (1 memory byte)	
 Integrated 	128 KB for code	Data blocks	Max. 511 (DB 0 reserved)	
	128 KB for data	• Size	Max. 64 Kbytes	
Load memory			,	
 Integrated 	256 KB RAM	Local data (can be set)	Max. 8 Kbytes	
 Expandable FEPROM 	With memory card (FLASH)	Preset	4 Kbytes	
	up to 64 MB		ocks	
 Expandable RAM 	With memory card (RAM) up to 64 MB	OBs	See instruction list	
Pooleup	Yes	• Size	Max. 64 Kbytes	
BackupWith battery	All data	Nesting depth		
,		Per priority class	24	
Without battery None Typical processing times		 Additionally in an error OB 	1	
	cessing times		May 050	
Processing times for		FBs	Max. 256	
Bit operations	0.1 μs	• Size	Max. 64 Kbytes	
Word instructions	0.1 μs	FCs	Max. 256	
 Integer math instructions 	0.1 μs	Size Address Areas	Max. 64 Kbytes	
 Floating-point math 	0.3 μs	Total I/O address area	(Inputs/Outputs)	
instructions	0.0 μο	 Of which distributed 	4 Kbytes/4 Kbytes incl. diagnostic addresses	
Timers/Counters	and Their Retentivity		for I/O intrerfaces etc.	
S7 counters	2048	MPI/DP interface	2 Kbytes/2 Kbytes	
• Retentivity can be set	From Z 0 to Z 2047	DP interface	4 Kbytes/4 Kbytes	
Preset	From Z 0 to Z 7	Process Image	4 Kbytes/4 Kbytes (can be	
 Counting range 	1 to 999		set)	
IEC counter	Yes	Preset	128 bytes/128 bytes	
• Туре	SFB	Number of partial	Max. 15	
S7 timers	2048	process images		
 Retentivity can be set 	From T 0 to T 2047	Consistent data	Max. 244 bytes	
Preset	No retentive timers	Digital channels	Max. 32768/Max. 32768	
Time range	10 ms to 9990 s	 Of which central 	Max. 32768/Max. 32768	
IEC timers	Yes	Analog channels	Max. 2048/Max. 2048	
 Type 	SFB	Of which central	Max. 2048/Max. 2048	
- iype				

Configuration			S7 Message Functions			
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	log fun	j on nctic	er of stations that can for message ons (e.g. WIN CC or FIC OP)	Max. 8	
Number of plug-in IMs (overall)	Max. 6	Sy		ol-related messages umber of messages	Yes	
	May G			0	May 510	
• IM 460	Max. 6		_	e rerai	Max. 512	
• IM 463-2	Max. 4		-	100 ms grid	None	
Number of DP masters			-	500 ms grid	Max. 256	
 Integrated 	2		-	1000 ms grid	Max. 256	
 Via IM 467 	Max. 4	•	Nu	umber of additional	1	
 Via CP 443-5 Extended 	Max. 10		va	llues per message		
IM 467 cannot be used with	the CP 443-5 Extended		_	With 100 ms grid	None	
IM 467 cannot be used with mode	the CP 443-1 EX40 in PN IO		_	With 500, 1000 ms grid	1	
Number of plug-in S5	Max. 6	Blo	ock-	related messages	Yes	
modules via adapter casing (in the central rack) Operable function modules and communication		•	AL ar	multaneously active _ARM_S/SQ blocks nd ALARM_D/DQ ocks	Max. 70	
processors				M 8 blocks	Yes	
• FM	Limited by the number of slots and the number of connections	•	Nı co	umber of ommunication jobs for _ARM_8 blocks and	Max. 300	
• CP 440	Limited by the number of slots		ble co	ocks for S7 ommunication (can be		
• CP 441	Limited by the number of connections	•	se De	et) efault	150	
 Profibus and Ethernet 	Max. 14	Pro	oce	ss control reports	Yes	
CPs incl. CP 443-5 Extended and IM 467		Nu	ımb	er of archives that g on simultaneously	4	
Ti	ime	(SFB 37 AR_SEND)				
Clock	Yes			Test and Star	tup Functions	
Buffered	Yes	Mo	onito	or/modify variable	Yes	
 Resolution Accuracy at Power off 	1 ms Deviation per day 1.7 s	•	Va	ariables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters	
 Power on 	Deviation per day 8.6 s	•	Nu	umber of variables	Max. 70	
Runtime meter	8	Fo	rce		Yes	
Number	0 to 7			ariables	Inputs/outputs, memory	
Value Range	0 to 32767 hours				markers, distributed	
Granularity	1 hour		~		inputs/outputs	
Retentive	Yes	•		uantity	Max. 64	
Time synchronization	Yes			block	Yes	
• In PLC, on MPI and DP	as master or slave	_	•	sequence	Yes	
		Dia	•	ostic buffer	Yes	
		•	Νι	umber of entries	Max. 400 (can be set)	
		•	Pr	reset	120	

Number of breakpoints

4

	ion Functions	1st Interface D	P Master Mode
Programming device/OP communication	Yes	 Utilities Programming 	Yes
Number of connectable OPs	15 without message processing, 8 with message	device/OP communication	
	processing	 Routing 	Yes
Number of connection resources for S7 connections via all	16, with one each of those reserved for PG and OP	 S7 basic communication S7 communication 	Yes
interfaces and CPs		 Constant bus cycle 	
Global data communication	Yes	time	Yes
 Number of GD circuits 	Max. 8	- SYNC/FREEZE	Yes
 Number of GD packages 		 Enable/disable DP slaves 	Yes
 Sender 	Max. 8	Transmission rates	Up to 12 Mbps
 Receiver 	Max. 16	 Number of DP slaves 	Max. 32
 Size of GD packages Of which consistent 	Max. 64 bytes 1 variable	Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
S7 basic communication	Yes	User data per DP slave	Max. 244 bytes inputs,
MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT		max.244 bytes outputs, max. 244 slots each with max. 128 bytes
DP Master ModeUser data per job	via SFC I_GET and I_PUT Max. 76 bytes	User data per DP slave	
 Of which consistent 	variable		
S7 communication	Yes	Note:	
User data per job	Max. 64 Kbytes	The accumulated	
- Of which consistent	······································	number of input bytes at the slots may not	
S5-compatible communication	via FC AG_SEND and AG RECV, max. via 10	exceed 244	
oommanioadon	CP 443-1 or 443-5)	The accumulated	
 User data per job Of which consistent 	Max. 8 Kbytes 240 bytes	number of output bytes at the slots may not	
Standard communication	Yes (via CP and loadable	exceed 244The maximum address	
(FMS)	FB)	area of the interface	
Inter	faces	(max. 2KB inputs /2 KB	
1st Int	erface	outputs) accumulated	
Type of interface	Integrated	by 32 slaves may not be exceeded	
Physical	RS 485/Profibus	1st Interface D	P Slave Mode
Isolated	Yes	You can only configure the Cl	
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA	if the CPU has several interfa	
Number of connection	MPI: 16	Utilities Monitor/modify	Vee
resources	DP: 16	 Monitor/modify 	Yes
Functi	onality	- Programming	Yes
• MPI	Yes	- Routing	Yes
PROFIBUS DP Int Interfee	DP master/DP slave e MPI Mode	• DDB (GSD) file	http://www.ad.siemens.de/o si_e/gsd
Utilities		Transmission rate	Up to 12 Mbps
 Programming 	Yes	Intermediate memory	244 bytes inputs/ 244 bytes outputs
device/OP communication		 Virtual slots 	Max. 32
 Routing 	Yes	 User data per address area 	Max. 32 bytes
 Global data communication 	Yes	 Of which consistent 	32 bytes
 S7 basic communication 	Yes		
 S7 communication 	Yes		
 Transmission rates 	Lin to 12 Mbns		

•

Transmission rates

Up to 12 Mbps

Type of interfaceIntegratedPhysicalRS 485/ProfibusIsolatedYesPower supply to interfaceMax. 150 mA(15 VDC to S0 VDC)Number of connectionNumber of connection16resourcesFunctionality• PROFIBUS DPDP master/DP slave• Utilities- Programming- RoutingYes- RoutingYes- S7 basicYes- Constant bus cycleYes- S7 basicYes- Constant bus cycleYes- S7 basicYes- Sr basicYes- Hendel(disable DPYes- StasseMax. 44- Number of DP slavesNumber of DP slavesMax. 44- Base load100 ms- Sr basic cord- Sr connunication- Sr basicMax. 44- The accumulatedMax. 44number of uput bytes- Sr basic- The accumulated- Sr basicnu				
Physical Isolated RS 485/Profibus • DPNRM_DG 8 Isolated Yes • DP_TOFOL 1 Pewer supply to interface resources Max. 150 mA DP_TOFOL 1 PROFIBUS DP Pm master/DP slave See instruction list PROFIBUS DP DP master/DP slave RD_REC 8 • Utilities - Programming device/OP communication Password protection - ST basic Yes - Souting Yes - Constant bus cylce Yes - Sortant bus cylce Yes - Constant bus cylce Yes - Sortant bus cylce Yes - Constant bus cylce Yes - Sortant bus cylce Yes - Transmission rates Up to 12 Mbps • Number of DP slaves Max. 4 Kbytes inputs, /4 kybres outputs, max. 244 bytes inputs, PA Sort 26, 127 • The accumulated number of suput bytes at the slots may not exceed 244 - Constant bus cylce time 'Yes Sort 26, 127 • The accumulated number dispecfications as for the 1st interface			PARM_MOD	1
Isolated Yes Power supply to interface Max. 150 mA Power supply to interface Max. 150 mA (IS VDC IG S0 VDC) See instruction list Number of connection 16 POPORESUS DP DP master/DP slave Programming Yes - Programming Yes - RD_REC - Routing Yes - Routing Yes - S7 Dasic Yes - Constant bus cylce Yes - ST Abasic Yes - SYNC/FREEZE Yes - Transmission rates Up to 12 Mbps Number of DP slaves Max. 4 Kbytes inputs / Address area Max. 4 Kbytes inputs / Address area Max. 4 Kbytes inputs / Ather actumutated Number of input bytes number of input bytes 15 ms Outing in maximum address Treasministion rates bytes Veriance DP slave The accumutated Max. 4 Kbytes inputs / number of input bytes 100 mersions Visce adult in terface Treasministion rates Very teacadult in terface Treasmining<	••	J. J		
Power supply to interface Max. 150 mA 1 (15 VDC to 30 VDC) 15 Number of connection 16 System function blocks Se instruction list (SFB) • PROFIBUS DP DP master/DP slave 8 • Utilities - RD_REC 8 • Utilities - Programming Yes - 8 - Programming in Yes - Cell synchronization time - - S7 basic Yes - Cilck synchronization time - S7 hasic Yes - Cilck synchronization time - S7 NC/FREEZE Yes - Constant bus cycle Max. 44 bytes inputs / - Vubre of DP slaves Max. 64 Constant bus cycle time Yes - Transmission rates Up to 12 Mbps Number of DP slaves Nax. 64 - Address area Max. 44 bytes inputs / 4 bytes inputs / 4 bytes inputs / 4 bytes outputs / 4 bytes inputs / 4 bytes outputs / 4 bytes inputs / 4 bytes inputs / 4 bytes inputs / 4 bytes outputs / 4 bytes inputs / 4 bytes outputs / 4 bytes inputs / 4 bytes input				-
(15 VDC to 30 VDC) Number of connection 16 resources Functionality • PROFIBUS DP DP master/DP slave 2 Molifilities - - Programming Yes - device/OP - communication - - Routing Yes - S7 constant bus cycle Yes - Constant bus cycle Yes - S7 communication Yes - Sync/FREEZE Yes - Number of DP slaves Max. 464 Max. 4 Kdytes outputsMax. 244 Softes achoutputs max. 244 Softes achoutputs A Krytes outputsMax. 244 Softes achoutputs A Krytes outputsMax. 244 Softes achoutputs Softes achoutputs A the slots may not exceed 244 Veriant consumption from more maximum address at the slots may not exceed 244 Softes achoutputs				
resources Functionality Functionality Programing Programming	(15 VDC to 30 VDC)		System function blocks	-
Functionality Functionality PROFIBUS DP DP master/DP slave RD_REC WR_REC WR_REC WR_REC User program protection Password protection Access to consistent data Yes Cirk synchronization time Base load 100 ms Transmission rates Up to 12 Mbps Number of DP slaves Max. 64 Address area Address area Address area Address area Address area Address area The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes are the slots may not exceed 244 The maximum address area of the interface (Technical specifications as for the 1st interface Programming Programming Inguage LAD, FBD, STL, SCL Instruction list Bracket leveis System functions (SFC) See instruction list System functions (SFC) See in		16	. ,	
 PROFIBUS DP DP master/DP slave 2nd Interface DP Master Mode WR_REC 8 WR_REC 8 WR_REC 8 User program protection Access to consistent data Yes in the process image CIR synchronization time Base load 100 ms S7 basic Yes communication Yes Constant bus cyclee Yes time SYNC/FREEZE Yes Enable/disable DP Yes Transmission rates Up to 12 Mbps Number of DP slaves Max. 4 Kbytes inputs / 4 Kbytes inputs / 4 Kbytes inputs max. 244 bytes outputsMax. 244 bytes out		ionality		
2nd Interface DP Master Mode • WH_REC 8 • Utilities - Programming device/OP communication Yes - Routing Yes - - Routing Yes - - S7 basic Yes - - S7 communication Yes - - S7 communication Yes - - S7 constant bus cylce time Yes - - SYNO/FREEZE Yes - - Enable/disable DP slaves Up to 12 Mbps Max. 64 Number of DP slaves Max. 64 Nax. 64 Number of DP slaves Max. 4 Koytes inputs / 4 Kbytes outputsMax. 244 bytes inputs, max. 244 bytes inputs, max. 244 bytes outputsMax. 244 bytes inputs, max. 244 bytes outputsMax. 2		-		8
 Utilities Utilities Programming Yes device/OP communication Routing Yes S7 basic Yes communication S7 basic Yes constant bus cylce Yes Transmission rates Vp to 12 Mbps Number of DP slaves Max. 64 Address area Wax. 64 Address area User data per DP slave Max. 64 Voytes outputs, max. 244 slots each with max. 128 bytes User data per DP slave The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface The accumulated number of suput bytes at the slots may not exceed 244 The maximum address area of the interface from max. 2KB inputs / 2 KB inpu			-	
 Programming Yes device/OP communication Routing Yes S7 basic Yes communication S7 basic Yes Communication Yes Constant bus cylce Yes time S7 constant bus cylce Yes S7 basic Yes Constant bus cylce Yes S7 basic Yes Constant bus cylce Yes S7 basic Yes Constant bus cylce Yes S7 basic Active Yes S7 basic Yes S7 basic Yes Constant bus cylce Yes S7 basic Yes S7 basic Yes Constant bus cylce Yes S7 basic Yes Yes Constant bus cylce Yes S7 basic Yes Yes Constant bus cylce Yes S7 basic Yes Yes Constant bus cylce Yes Yes Yes Constant bus cylce Yes Yes Yes Yes Yes Yes Yes Yes Yes Ye			_	-
device/OP in the process image communication CiR synchronization time Base load 100 ms S7 basic Yes S7 basic Yes Communication Time per I/O byte 200 µs Constant bus cylce Yes Constant bus cylce Yes SYNC/FREEZE Yes Transmission rates Up to 12 Mbps Number of DP slaves Max. 64 Address area Max. 64 Address area Max. 4K bytes inputs / 4 Vites outputs, max. 244 bytes outputs, max. 244 slots each with max. 128 bytes The accumulated number of input bytes number of output bytes 1 at the slots may not exceed 244 The maximum address area of the interface In the groamming Programming Frogramming Programming Frogramming Programming language LAD, FBD, STL, SCL Instruction set See instruction list System functions (SFC) See instruction list Number of SFCs active at SVetor 15 VDC		Yes		·
- Routing Yes - S7 basic Yes - S7 basic Yes - S7 communication Yes - Constant bus cylce Yes - Constant bus cylce Yes - Enable/disable DP Yes - Enable/disable DP Yes - Transmission rates Up to 12 Mbps Number of DP slaves Max. 4 Kbytes inputs / 4 Kbytes outputs, max.244 bytes inputs, max.244 bytes outputs, max.244 by		100		100
 So that So the second So th	communication		CiR synchro	nization time
communication Yes - S7 communication Yes - Clock synchronoism - SYNC/FREEZE Yes - SYNC/FREEZE Yes - SYNC/FREEZE Yes - Enable/disable DP Yes - Transmission rates Up to 12 Mbps Number of DP slaves Max. 44 Max. 44 Address area Max. 4 Kbytes inputs / - 4 Kbytes outputs!Max. 244 bytes outputs!max. 244 vites outputs with max. 128 bytes bytes Dimensions 0.5 ms without use of SFC 126, 127 see manual Clock Synchronism 25x290x219 WxHxD (mm) 25x290x219 WxHxD (mm) 25x290x219 Weight approx. 0,72 kg Current consumption from the S7-400 bus (5 VDC) The acoumulated number of output bytes area of the interface number of output bytes area of the interface Programming Programming Programming Programming Programming Programming Ab, FBD, STL, SCL Instruction set S	0	Yes	Base load	100 ms
 S7 communication Yes Clock synchronism Clock synchronism User data per Clock SynC/FREEZE Yes Transmission rates Up to 12 Mbps Max. 64 Address area User data per DP slave Max. 4 Kbytes outputs/ax.244 bytes inputs / a Kbytes outputs, max.244 Synchronism User data per DP slave The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes area to the interface (max. 2KB inputs / 2 KB outputs / 2 kB		Yes	Time per I/O byte	200 µs
- Constant bus cylce Yes Max. 244 bytes - SYNC/FREEZE Yes Max. 124 bytes - Enable/disable DP Yes Max. 64 Number of DP slaves Max. 64 Max. 64 Address area Max. 4 Kbytes inputs / 4 Kbytes inputs / 4 Kbytes inputs, max. 244 bytes inputs, max. 240 bytes inputs, max. 244 bytes inputs, max. 244 bytes inputs,			Clock sy	nchronism
time - SYNC/FREZE Yes - Enable/disable DP Yes - Enable/disable DP Yes - Transmission rates Up to 12 Mbps Number of DP slaves Max. 64 Constant bus cylce time Yes - Address area Max. 4 Kbytes inputs / 4 Kbytes outputsMax. 244 bytes outputsmax. 244 bytes outputsmax. 244 bytes outputsmax. 244 slots each with max. 128 bytes Dimensions - The accumulated number of output bytes at the slots may not exceed 244 Stots required 1 - The accumulated number of output bytes at the slots may not exceed 244 Stots required 1 - The accumulated number of output bytes at the slots may not exceed 244 Stots required 1 - The maximum address area of the interface (max. 2KB inputs /2 KB outputsmay not by 32 slaves may not be exceeded State Stots may not exceed 244 Stots required 1 Programming Programming Fredenical specifications as for the 1st interface The maximum address area of the interface Stots area of the interface The Actup type Stot Actup the Stots as 0 µA Technical specifications as for the 1st interface Programming The Stot Pay as 0 µA Programming language LAD, FBD, STL, SCL				Max. 244 bytes
 SYNC/FREZZ Yes Enable/disable DP Yes Transmission rates Up to 12 Mbps Number of DP slaves Address area User data per DP slave Wax. 4 Kbytes inputs / 4 Kbytes outputs/max. 244 bytes outputs, max. 244 slots each with max. 128 bytes The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Znd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list System functions (SFC) See instruction list Number of SFCs active at 		165	,	
 Enable/disable DP slaves Transmission rates Up to 12 Mbps Number of DP slaves Address area Max. 4 Kbytes inputs / 4 Kbytes outputsMax. 244 bytes outputsMax. 244 slots each with max. 128 bytes The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FED, STL, SCL Instruction set See instruction list Number of SFCs active at 		Yes		0 11
 Transmission rates Transmission rates Up to 12 Mbps Number of DP slaves Max. 64 Address area User data per DP slave Wax. 4 Kbytes inputs / 4 Kbytes outputs, max. 244 bytes outputs, max. 244 bytes outputs, max. 244 The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs / 2 KB outputs) accumulated by 2 slaves may not be exceededed 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Max. 64 Nax. 4 Kbytes inputs / 4 Kbytes outputs, accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface be exceeded 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Max es a substruction list Number of SFCs active at 	- Enable/disable DP			
 Number of DP slaves Address area User data per DP slave Wax. 4 Kbytes inputs / 4 Kbytes outputsMax. 244 bytes inputs, max. 244 slots each with max. 128 bytes The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs / 2 KB outputs) accumulated putputs) accumulated programming Znd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Number of SFCs active at 		Lin to 10 Million	Constant bus cylce time	Yes
 Address area User data per DP slave Wax. 4 Kbytes inputs / 4 Kbytes inputs, max.244 bytes inputs, max.244 slots each with max. 128 bytes The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The accumulated number of output bytes area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded 25.290×219 WxHxD (mm) Slots required Weight approx. 0,72 kg Current consumption from the S7-400 bus (5 VDC) Max. 1.2 A Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface. Backup current Typ. 350 µA maximum backup time See manual Module Specifications, chapter 3. Incoming supply of external backup voltage to the CPU Power loss Typ. 4.5 W 		· ·	Shortest clock pulse	1.5 ms
 User data per DP slave 4 Kbytes outputs/max. 244 bytes outputs, max. 244 slots each with max. 128 bytes The accumulated number of input bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list System functions (SFC) See instruction list Number of SFCs active at 				
bytes outputs, max. 244 slots each with max. 128 bytes Synchronism • The accumulated number of input bytes at the slots may not exceed 244 · Mounting dimensions 25×290×219 • The accumulated number of output bytes at the slots may not exceed 244 · Mounting dimensions 25×290×219 • The accumulated number of output bytes at the slots may not exceed 244 · Voltages, Currents • The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded · Voltages, Currents • The communated rest area of the interface by 32 slaves may not be exceeded · Current consumption from (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded · Typ. 350 µA Max. 890 µA • Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Bracket levels 8 · Noch in the CPU System functions (SFC) See instruction list · Noch in the CPU Number of SFCs active at · See instruction list · Noch in the CPU		4 Kbytes outputsMax. 244	soo manual Clock	SFC 126, 127
bytes Dimensions • The accumulated number of input bytes at the slots may not exceed 244 Mounting dimensions 25×290×219 • The accumulated number of output bytes at the slots may not exceed 244 1 approx. 0,72 kg • The accumulated number of output bytes at the slots may not exceed 244 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface. Total current consumption of the components connected to the MPI/DP interfaces, with a maximu of 150 mA per interface Programming Programming Backup current Typ. 350 µA Max. 890 µA Programming language LAD, FBD, STL, SCL Instruction set See instruction list Incoming supply of external backup voltage to the CPU 5 VDC to 15 VDC System functions (SFC) See instruction list Incoming supply of external backup voltage to the CPU 5 VDC to 15 VDC Power loss Typ. 4.5 W		bytes outputs, max. 244		
• The accumulated number of input bytes at the slots may not exceed 244 > Mounting dimensions 25×290×219 • The accumulated number of output bytes at the slots may not exceed 244 > I • The accumulated number of output bytes at the slots may not exceed 244 > I • The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Voltages, Currents • Thermaximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Total current consumption the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface. Total current consumption of the components connected to the MPI/DP interfaces, with a maximu of 150 mA per interface Programming Backup current Typ. 350 μA Max. 890 μA Programming language LAD, FBD, STL, SCL Instruction set See instruction list Bracket levels 8 Incoming supply of external backup voltage to the CPU 5 VDC to 15 VDC Power loss Typ. 4.5 W				nsions
at the slots may not exceed 244Weightapprox. 0,72 kg• The accumulated number of output bytes at the slots may not exceed 244Voltages, Currents• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededTotal current consumption from the S7-400 bus (5 VDC)Total current consumption of the components• The examulated by 32 slaves may not be exceededCurrent consumption from the S7-400 bus (24 VDC)Total current consumption of the components• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededTotal current consumption of the components• The cPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.Total current consumption of 150 mA per interface MAX. 890 µA• Programming Programming languageLAD, FBD, STL, SCL Instruction setTyp. 350 µA Max. 890 µAIncoming supply of external backup voltage to the CPU5 VDC to 15 VDCPower lossTyp. 4.5 W	The accumulated	bytoo		25×290×219
exceed 244Weightapprox. 0,72 kg• The accumulated number of output bytes at the slots may not exceed 244Voltages, Currents• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededCurrent consumption from s7-400 bus (5 VDC)Total current consumption of the components connected to the MPI/DP interfaces, with a maximu of 150 mA per interface2nd Interface DP Slave ModeTechnical specifications as for the 1st interfaceTyp. 350 μA Max. 890 μAProgramming Brogramming languageLAD, FBD, STL, SCL Instruction setSee instruction listIncoming supply of external backup voltage to the CPU5 VDC to 15 VDCNumber of SFCs active atSee instruction listProgramingTyp. 4.5 W			Slots required	1
 The accumulated number of output bytes at the slots may not exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming language LAD, FBD, STL, SCL Instruction set See instruction list Programming language LAD, FBD, STL, SCL Instruction set See instruction list System functions (SFC) See instruction list Voltages, Currents Voltages, Currents Current consumption from the S7-400 bus (5 VDC) Max. 1.2 A Current consumption from the S7-400 bus (24 VDC) The CPU does not connected to the MPI/DP interface. Backup current Typ. 350 μA Max. 890 μA maximum backup time See manual Module Specifications, chapter 3. Incoming supply of external backup voltage to the CPU Power loss Typ. 4.5 W 			Weight	approx. 0,72 kg
number of output bytes at the slots may not exceed 244Current consumption from S7-400 bus (5 VDC)Typ. 1.0 A Max. 1.2 A• The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededCurrent consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.Total current consumption of the components connected to the MPI/DP interfaces, with a maximu of 150 mA per interfaceImage: Technical specifications as for the 1st interfaceTyp. 350 μA Max. 890 μAProgramming languageLAD, FBD, STL, SCL Instruction setSee instruction listInstruction setSee instruction listIncoming supply of external backup voltage to the CPUSystem functions (SFC)See instruction listIncoming supply of external backup voltage to the CPUNumber of SFCs active atSee instruction listTyp. 4.5 W			Voltages	, Currents
 Exceed 244 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Pracket levels 8 System functions (SFC) See instruction list Number of SFCs active at 	number of output bytes			Тур. 1.0 А
 The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded 2nd Interface DP Slave Mode Technical specifications as for the 1st interface Programming Programming language LAD, FBD, STL, SCL Instruction set See instruction list Pracket levels 8 System functions (SFC) See instruction list Number of SFCs active at 			S7-400 bus (5 VDC)	Max. 1.2 A
area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededthe S/-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.of the components connected to the MPI/DP interfaces, with a maximu of 150 mA per interface2nd Interface DP Slave ModeBackup current MPI/DP interface.Typ. 350 μA Max. 890 μAProgramming Instruction set Bracket levelsSee instruction list 8Incoming supply of external backup voltage to the CPU5 VDC to 15 VDCNumber of SFCs active atSee instruction listPower lossTyp. 4.5 W				Total current consumption
(max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceededconsume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.interfaces, with a maximu of 150 mA per interface2nd Interface DP Slave ModeBackup currentTyp. 350 μA Max. 890 μATechnical specifications as for the 1st interfaceMax. 890 μAProgramming languageLAD, FBD, STL, SCLIncoming supply of external backup voltage to the CPU5 VDC to 15 VDCInstruction set8See instruction listIncoming supply of external backup voltage to the CPU5 VDC to 15 VDCSystem functions (SFC)See instruction listPower lossTyp. 4.5 W			,	•
Outputs) accumulated 24 V, and it only makes this voltage available at the MPI/DP interface. of 150 mÅ per interface 2nd Interface DP Slave Mode Backup current Typ. 350 μA Technical specifications as for the 1st interface Max. 890 μA Programming language LAD, FBD, STL, SCL maximum backup time See manual Module Specifications, chapter 3. Instruction set See instruction list Incoming supply of external backup voltage to the CPU 5 VDC to 15 VDC System functions (SFC) See instruction list Power loss Typ. 4.5 W				interfaces, with a maximum
be exceeded Voltage available at the MPI/DP interface. 2nd Interface DP Slave Mode MPI/DP interface. Technical specifications as for the 1st interface Backup current Typ. 350 μA Programming Max. 890 μA Max. 890 μA Programming language LAD, FBD, STL, SCL Instruction set See instruction list Bracket levels 8 Incoming supply of external backup voltage to the CPU 5 VDC to 15 VDC System functions (SFC) See instruction list Power loss Typ. 4.5 W				of 150 mA per interface
2nd Interface DF Slave Mode Typ. 350 μA Technical specifications as for the 1st interface Max. 890 μA Programming language LAD, FBD, STL, SCL Instruction set See instruction list Bracket levels 8 System functions (SFC) See instruction list Number of SFCs active at See instruction list				
Technical specifications as for the 1st interface Max. 890 μA Programming Max. 890 μA Programming language LAD, FBD, STL, SCL Instruction set See instruction list Bracket levels 8 System functions (SFC) See instruction list Number of SFCs active at See instruction list	2nd Interface I	DP Slave Mode		Tvp. 350 µA
ProgrammingMaximum backup timeSee manual Module Specifications, chapter 3.Programming languageLAD, FBD, STL, SCLIncoming supply of external backup voltage to the CPUSvDC to 15 VDCInstruction set8backup voltage to the CPUTyp. 4.5 WSystem functions (SFC)See instruction listPower lossTyp. 4.5 W	Technical specifications as for	or the 1st interface		•• •
Programming languageLAD, FBD, STL, SCLSpecifications, chapter 3.Instruction setSee instruction listIncoming supply of external backup voltage to the CPU5 VDC to 15 VDCSystem functions (SFC)See instruction listPower lossTyp. 4.5 W	Progra	imming	maximum backup time	•
Bracket levels 8 System functions (SFC) See instruction list Number of SFCs active at Visit of Section 10 visit of V	Programming language	LAD, FBD, STL, SCL		Specifications, chapter 3.3
System functions (SFC) See instruction list Power loss Typ. 4.5 W Number of SFCs active at	Instruction set	See instruction list		5 VDC to 15 VDC
Number of SFCs active at	Bracket levels	8	backup voltage to the CPU	
	System functions (SFC)	See instruction list	Power loss	Тур. 4.5 W
	Number of SFCs active at the same time per segment			
• DP_SYC_FR 2	DP_SYC_FR	2		
• D_ACT_DP 4		4		
• RD_REC 8		8		
• WR_REC 8	-	8		
• WR_PARM 8	—	8		

6.3 Technical Specifications of the CPU 414-2; (6ES7414-2XG04-0AB0)

CPU and Version		Data Areas and	Their Retentivity
MLFB Firmware version Associated programming package	6ES7414-2XG04-0AB0 V 4.0.0 As of STEP7 5.2 SP1 HF3 with HW-Update	Total retentive data areas (including memory bits; times; counts) Memory markers	Total working and load memory (with backup battery) 8 Kbytes
Me	emory	 Retentivity can be set 	From MB 0 to MB 8191
Working memory	-	 Preset retentivity 	From MB 0 to MB 15
 Integrated 	256 Kbytes for code	Clock memories	8 (1 memory byte)
	256 Kbytes for data	Data blocks	Max. 4095 (DB 0 reserved)
Load memory	-	Size	Max. 64 Kbytes
 Integrated 	256 Kbytes RAM	Local data (can be set)	Max. 16 Kbytes
Expandable FEPROM	With memory card (FLASH)	Preset	8 Kbytes
	up to 64 Mbytes	Ble	ocks
 Expandable RAM 	With memory card (RAM)	OBs	See instruction list
	up to 64 Mbytes	Size	Max. 64 Kbytes
Backup with battery	Yes, all data	Nesting depth	
	essing Times	 Per priority class 	24
Processing times for		Additionally in an error	1
 Bit operations 	0.06 µs	OB	
 Word instructions 	0.06 µs	FBs	Max. 2048
 Integer math 	0.06 µs	Size	Max. 64 Kbytes
instructions	0.10	FCs	Max. 2048
 Floating-point math instructions 	0.18µs	Size	Max. 64 Kbytes
	and Their Retentivity		(Inputs/Outputs)
S7 counters	2048	Total I/O address area	8 Kbytes/8 Kbytes
 Retentivity can be set 	From Z 0 to Z 2047	Of which distributed	incl. diagnostic addresses for I/O interfaces, etc.
 Preset 	From Z 0 to Z 7	MPI/DP interface	. ,
 Counting range 	1 to 999	DP interface	2 Kbytes/2 Kbytes
IEC counter	Yes		6 Kbytes/6 Kbytes
Type	SFB	Process Image	8 Kbytes/8 Kbytes (can be set)
S7 timers	2048	Preset	256 bytes/256 bytes
 Retentivity can be set 	From T 0 to T 2047	 Number of partial 	Max. 15
 Preset 	No retentive timers	process images	
 Time range 	10 ms to 9990 s	Consistent data	Max. 244 bytes
IEC timers	Yes	Digital channels	Max. 65536/Max. 65536
	SFB	 Of which central 	Max. 65536/Max. 65536
• Type	0.5	Analog channels	Max. 4096/Max. 4096
		 Of which central 	Max. 4096/Max. 4096

Config	Configuration		e Functions
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Number of plug-in IMs	Max. 6	Symbol-related messages	Yes
(overall)		Number of messages	
• IM 460	Max. 6	– Overall	Max. 512
 IM 463-2 	Max. 4	– 100 ms grid	Max. 128
Number of DP masters		– 500 ms grid	Max. 256
 Integrated 	2	– 1000 ms grid	Max. 512
 Via IM 467 	Max. 4	Number of additional	
• Via CP 443-5 Extended	Max. 10	values per message	
IM 467 cannot be used with	the CP 443-5 Extended	– With 100 ms grid	Max. 1
IM 467 cannot be used with mode	the CP 443-1 EX40 in PN IO	 With 500 – 1000 ms grid 	Max. 10
Number of plug-in S5	Max. 6	Block-related messages	Yes
modules via adapter casing (in the central rack) Operable function modules and communication		Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 100
processors		ALARM 8 blocks	Yes
• FM	Limited by the number of slots and the number of connections	 Number of communication jobs for ALARM 8 blocks and 	Max. 600
• CP 440	Limited by the number of slots	blocks for S7 communication (can be	
• CP 441	Limited by the number of connections	set) • Preset	300
 Profibus and Ethernet 	Max. 14	Process control reports	Yes
CPs, LANs incl. CP 443-5 Extended and IM 467		Number of archives that can log on simultaneously (SFB 37 AR SEND)	16
Ti	me	Test and Startup Functions	
Clock	Yes	Monitor/modify variable	Yes
 Buffered Resolution Accuracy at Bource off 	Yes 1 ms	Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
 Power off 	Deviation per day 1.7 s	Number of variables	Max. 70
- Power on	Deviation per day 8.6 s	Force	Yes
Runtime meter	8 0 to 7	Variables	Inputs/outputs, memory
Number	0 to 7		markers, distributed
Value Range	0 to 32767 hours		inputs/outputs
Granularity	1 hour	Number of variables	Max. 256
Retentive	Yes	Status block	Yes
Time synchronization	Yes	Single sequence	Yes
In PLC, on MPI and DP	as master or slave	Diagnostic buffer	Yes
		Number of entries	Max. 400 (can be set)
		Preset	120
		Number of breakpoints	4

Communicat	ion Functions	1st l	nterface D	P Master Mode
Programming device/OP communication	Yes	 Utilities Programn 	nina	Yes
Number of connectable OPs	31 without message processing, 8 with message	device/OF communic	D	
	processing	 Routing 		Yes
Number of connection resources for S7 connections via all	32, with one each of those reserved for PG and OP	 S7 basic communic 	cation	Yes
interfaces and CPs		 S7 commi 	unication	Yes
Global data communication	Yes	- Constant	bus cycle	Yes
Number of GD circuits	Max. 8	time		
 Number of GD packages 		 SYNC/FR Enable/dis 		Yes Yes
– Sender	Max. 8	slaves Transmission 		
 Receiver 	Max. 16	Tranornoolorr		Up to 12 Mbps
 Size of GD packages 	Max. 64 bytes	Number of DF		Max. 32
 Of which consistent 	1 variable	Address area		Max. 2 Kbytes inputs/ 2 Kbytes outputs
S7 basic communication	Yes	User data per	DP slave	Max. 244 bytes inputs,
MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT			max.244 bytes outputs, max. 244 slots each with
DP Master Mode	via SFC I GET and I PUT	User data per	DP slave	max. 128 bytes
 User data per job 	Max. 76 bytes			
 Of which consistent 	1 variable	Note:		
S7 communication	Yes	The accumula		
 User data per job 	Max. 64 Kbytes	number of inp		
 Of which consistent 		at the slots ma	ay not	
S5-compatible	via FC AG SEND and	The accumula	ated	
communication	AG_RECV, max. via 10 CP 443-1 or 443-5)	number of out at the slots ma	put bytes	
 User data per job 	Max. 8 Kbytes	exceed 244The maximum	addroop	
 Of which consistent 	240 bytes	area of the inte		
Standard communication (FMS)	Yes (via CP and loadable FB)	(max. 2KB inp outputs) accur	mulated	
	faces	by 32 slaves r	nay not	
	erface		Interface [DP Slave Mode
Type of interface	Integrated			PU once as a DP slave ever
Physical	RS 485/Profibus	if the CPU has sev	0	
Isolated	Yes	Utilities		
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA	– Monitor/m		Yes
Number of connection resources	MPI: 32 DP: 16	- Programn	ining	Yes Yes
	onality	- Routing		
MPI	Yes	DDB (GSD) fil	IE	http://www.ad.siemens.de/o
PROFIBUS DP	DP master/DP slave	Transmission	rate	Up to 12 Mbps
1st Interfac	e MPI Mode	Intermediate n		244 bytes inputs/ 244 bytes outputs
Utilities		– Address a	areas	Max. 32
Programming device/OP	Yes	 User data address a 	per	Max. 32 bytes
communication			consistent	32 bytes
- Routing	Yes			
 Global data communication 	Yes			
 S7 basic communication 	Yes			
 S7 communication 	Yes			
· · · · ·	Into 10 Mhore			

•

Transmission rates

Up to 12 Mbps

	terface	D_ACT_DP	4
Type of interface		RD_REC	8
Physical	RS 485/Profibus	WR_REC	8
Isolated	Yes	WR_PARM	8
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA	PARM_MODWR DPARM	1 2
Number of connection	16	DPNRM DG	8
resources		RDSYSST	1 to 8
	onality	DP TOPOL	1
 PROFIBUS DP 	DP master/DP slave	System function blocks	See instruction list
	P Master Mode	(SFB)	
 Utilities Programming 	Yes	Number of SFBs active at the same time	
device/OP communication		RD_REC	8
	Yes	WR_REC	8
 Routing S7 basic 	Yes	User program protection	Password protection
communication		Access to consistent data in the process image	Yes
 S7 communication 	Yes		nization time
 Constant bus cycle 	Yes	Base load	100 ms
time – SYNC/FREEZE	Yes	Time per I/O byte	80 µs
 – STNC/FREEZE – Enable/disable DP 	Yes	Clock sy	nchronism
slaves	165	User data per clock synchronous slave	Max. 244 bytes
 Transmission rates 	Up to 12 Mbps	Maximum number of bytes	The following applies:
 Number of DP slaves 	Max. 96	and slaves in a process	number of bytes / 100 +
Address area	Max. 6 Kbytes inputs/6 Kbytes outputs	image partition	number of slaves < 26
• User data per DP slave	Max. 244 bytes inputs,	Constant bus cycle time	Yes
• User data per DP slave	max.244 bytes outputs,	Shortest clock pulse	1 ms
	max. 244 slots each with max. 128 bytes	See manual Clock Synchronism	0.5 ms without use of SFC 126, 127
Note:		Dime	nsions
The accumulated		Mounting dimensions W×H×D (mm)	25×290×219
number of input bytes at the slots may not		Slots required	1
exceed 244		Weight	approx. 0,72 kg
The accumulated		Voltages	, Currents
number of output bytes at the slots may not		Current consumption from	Тур. 1.0 А
exceed 244		S7-400 bus (5 VDC)	Max. 1.2 A
• The maximum address		Current consumption from	Total current consumption
area of the interface (max. 2KB inputs /2 KB		the S7-400 bus (24 VDC) The CPU does not	of the components connected to the MPI/DP
outputs) accumulated		consume any current at	interfaces, with a maximum
by 32 slaves may not		24 V, and it only makes this	of 150 mA per interface
be exceeded		voltage available at the	
	DP Slave Mode	MPI/DP interface.	
As for the 1st interface		Backup current	Typ. 550 μA
0	Imming	movimum hookur time	Max. 1530 µA
Programming language Instruction set	LAD, FBD, STL, SCL See instruction list	maximum backup time	See manual <i>Module</i> <i>Specifications</i> , chapter 3.3
Bracket levels	8	Incoming supply of external	5 VDC to 15 VDC
System functions (SFC)	See instruction list	backup voltage to the CPU	
System function blocks (SFB)	See instruction list	Power loss	Тур. 1,5 W
(SFB) Number of SFCs active at			
the same time for every strand			

2

DP_SYC_FR

•

6.4 Technical Specifications of the CPU 414-3; (6ES7414-3XJ04-0AB0)

CPU and Version		Data Areas and	Their Retentivity
MLFB Firmware version Associated programming package	6ES7414-3XJ04-0AB0 V 4.0.0 As of STEP 7 5.2 SP1 HF3 with HW-Update	Total retentive data areas (including memory bits; times; counts) Memory markers	Total working and load memory (with backup battery) 8 Kbytes
M	emory	Retentivity can be set	From MB 0 to MB 8191
Working memory		 Preset retentivity 	From MB 0 to MB 15
 Integrated 	700 Kbytes for code	Clock memories	8 (1 memory byte)
	700 Kbytes for data	Data blocks	Max. 4095 (DB 0 reserved)
Load memory	-	Size	Max. 64 Kbytes
 Integrated 	256 Kbytes RAM	Local data (can be set)	Max. 16 Kbytes
Expandable FEPROM	With memory card (FLASH)	Preset	8 Kbytes
	up to 64 Mbytes	Ble	ocks
 Expandable RAM 	With memory card (RAM)	OBs	See instruction list
	up to 64 Mbytes	• Size	Max. 64 Kbytes
Backup with battery	Yes, all data	Nesting depth	
	essing Times	 Per priority class 	24
Processing times for		Additionally in an error	1
 Bit operations 	0.06µs	OB	
 Word instructions 	0.06 µs	FBs	Max. 2048
 Integer math 	0.06 µs	Size	Max. 64 Kbytes
instructions	0.40	FCs	Max. 2048
 Floating-point math instructions 	0.18µs	Size	Max. 64 Kbytes
	and Their Retentivity		(Inputs/Outputs)
S7 counters	2048	Total I/O address area	8 Kbytes/8 Kbytes
 Retentivity can be set 	From Z 0 to Z 2047	Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
 Preset 	From Z 0 to Z 7	MPI/DP interface	. ,
 Counting range 	1 to 999	DP interface	2 Kbytes/2 Kbytes
IEC counter	Yes		6 Kbytes/6 Kbytes
 Type 	SFB	Process Image	8 Kbytes/8 Kbytes (can be set)
S7 timers	2048	Preset	256 bytes/256 bytes
 Retentivity can be set 	From T 0 to T 2047	Number of partial	Max. 15
 Preset 	No retentive timers	process images	
 Time range 	10 ms to 9990 s	Consistent data	Max. 244 bytes
IEC timers	Yes	Digital channels	Max. 65536/Max. 65536
	SFB	 Of which central 	Max. 65536/Max. 65536
• Type	0.5	Analog channels	Max. 4096/Max. 4096
		 Of which central 	Max. 4096/Max. 4096

Configuration		S7 Message Functions	
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Number of plug in IMe	(, , , , , , , , , , , , , , , , , , ,	Symbol-related messages	Yes
Number of plug-in IMs (overall)	Max. 6	Number of messages	
• IM 460	Max. 6	– Overall	Max. 512
 IM 463-2 	Max. 4	- 100 ms grid	Max. 128
Number of DP masters	Max. 4	– 500 ms grid	Max. 256
	0	U U	Max. 512
integrated	2	– 1000 ms grid	
 Via IF 964-DP Via IM 467 	1 Maria 4	Number of additional	
 Via IM 467 Via OD 448 5 Extended 	Max. 4	Values per message	Max. 1
• Via CP 443-5 Extended		- With 100 ms grid	
	the CP 443-5 Extended the CP 443-1 EX40 in PN IO	 With 500 to 1000 ms grid 	Max. 10
mode		Block-related messages	Yes
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6	Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ	Max. 100
Operable function modules and communication		blocks	Vee
processors		ALARM-8 blocks	Yes
∙ FM	Limited by the number of slots and the number of connections	 Number of communication jobs for ALARM-8 blocks and blocks for S7 	Max. 600
• CP 440	Limited by the number of slots	communication (can be set)	
• CP 441	Limited by the number of connections	Preset	300
 Profibus and Ethernet 	Max. 14	Process control reports	Yes
CPs incl. CP 443-5 Extended and IM 467		Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16
Ti	ime	Test and Startup Functions	
Clock	Yes	Monitor/modify variable	Yes
 Buffered Resolution Accuracy at 	Yes 1 ms	Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
 Power off 	Deviation per day 1.7 s	Number of variables	Max. 70
 Power on 	Deviation per day 8.6 s	Force	Yes
Runtime meter	8	Variables	Inputs/outputs, memory
Number	0 to 7		markers, distributed
 Value Range 	0 to 32767 hours		inputs/outputs
 Granularity 	1 hour	Number of variables	Max. 256
Retentive	Yes	Status block	Yes
	Yes	Single sequence	Yes
Time synchronization		[]	
 In PLC, on MPI, DP 	as master or slave	Diagnostic buffer	Yes
	as master or slave	Diagnostic buffer Number of entries Preset	Yes Max. 3200 (can be set) 120

	on Functions		DP Master Mode
Programming device/OP communication	Yes	 Utilities Programming 	Yes
Number of connectable OPs	31 without message processing, 8 with message processing	device/OP communication	
Number of connection	32, with one each of those	- Routing	Yes
resources for S7 connections via all	reserved for PG and OP	- S7 basic communication	Yes
interfaces and CPs		 S7 communication 	Yes
Global data communication	Yes	 Constant bus cycle time 	Yes
 Number of GD circuits 	Max. 8	– SYNC/FREEZE	Yes
 Number of GD packages 		- Enable/disable DP	Yes
 Sender 	Max. 8	slaves	Lin to 10 Minus
 Receiver 	Max. 16	Transmission rates	Up to 12 Mbps
 Size of GD packages 	Max. 64 bytes	 Number of DP slaves Address area 	Max. 32 May: 0 K/butas insuts/0
 Of which consistent 	1 variable	 Address area 	Max. 2 Kbytes inputs/2 Kbytes outputs
S7 basic communication	Yes	User data per DP slave	Max. 244 bytes inputs,
MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT	User data per DP slave	max.244 bytes outputs, max. 244 slots each with
DP Master Mode	via SFC I_GET and I_PUT		max. 128 bytes
 User data per job 	Max. 76 bytes	Note:	
 Of which consistent 	1 variable	The accumulated	
S7 communication	Yes	number of input bytes	
 User data per job 	Max. 64 Kbytes	at the slots may not exceed 244	
 Of which consistent 	1 variable (462 bytes)	 The accumulated 	
S5-compatible	via FC AG_SEND and	number of output bytes	
communication	AG_RECV, max. via 10 CP 443-1 or 443-5)	at the slots may not exceed 244	
 User data per job 	Max. 8 Kbytes	The maximum address	
 Of which consistent 	240 bytes	area of the interface (max. 2KB inputs /2 KB	
Standard communication (FMS)	Yes (via CP and loadable FB)	outputs) accumulated by 32 slaves may not	
	faces	be exceeded	
	erface		DP Slave Mode
Type of interface	Integrated	You can only configure the C if the CPU has several interf	CPU once as a DP slave even
Physical	RS 485/Profibus		acco.
Isolated	Yes	Utilities	
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA	– Monitor/modify	Yes Yes
Number of connection	MPI: 32	- Programming	Yes
resources	DP: 16	- Routing	
	onality	DDB (GSD) file	http://www.ad.siemens.de/ csi e/gsd
• MPI	Yes	Transmission rate	Up to 12 Mbps
PROFIBUS DP 1st Interfac	DP master/DP slave e MPI Mode	Intermediate memory	244 bytes inputs/ 244 bytes outputs
Utilities		 virtual slots 	Max. 32
 Programming device/OP 	Yes	 User data per address area 	Max. 32 bytes
communication		 Of which consistent 	32 bytes
 Routing 	Yes		•
 Global data 	Yes		
communication – S7 basic			
communication	Yes		
 S7 communication Transmission rates 	Yes Un to 12 Mbns		

2nd Ir	iterface	Number of SFCs active at	
Type of interface	Integrated	the same time for every	
Physical	RS 485/Profibus	strand	
Isolated	Yes	DP_SYC_FR	2
Power supply to interface	Max. 150 mA	D_ACT_DP	4
(15 VDC to 30 VDC)		RD_REC	8
Number of connection	16	WR_REC	8
resources		• WR_PARM	8
Funct	ionality	PARM_MOD	1
 PROFIBUS DP 	DP master/DP slave	WR_DPARM	2
2nd Interface I	DP Master Mode	 DPNRM_DG 	8
Utilities		RDSYSST	1 to 8
 Programming 	Yes	DP_TOPOL	1
device/OP communication		System function blocks (SFB)	See instruction list
 Routing 	Yes	Number of SFBs active at	
 S7 basic 	Yes	the same time	_
communication		RD_REC	8
 S7 communication 	Yes	WR_REC	8
 Constant bus cycle 	Yes	User program protection	Password protection
time – SYNC/FREEZE	Yes	Access to consistent data in the process image	Yes
 Enable/disable DP 	Yes	CiR synchro	nization time
slaves		Base load	100 ms
 Transmission rates 	Up to 12 Mbps	Time per I/O byte	80 µs
 Number of DP slaves 	Max. 96	Clock sy	nchronism
 Address area 	Max. 6 Kbytes inputs/6 Kbytes outputs	User data per clock synchronous slave	Max. 244 bytes
User data per DP slaveUser data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes	Maximum number of bytes and slaves in a process image partition	The following applies: Numer of bytes/100 + number of slaves <16
		Constant bus cycle time	Yes
Note:		Shortest clock pulse	1 ms
• The accumulated number of input bytes			0.5 ms without use of SFC 126, 127
at the slots may not exceed 244		Longest clock pulse	32 ms
The accumulated number of output bytes		see <i>Clock Synchronism</i> manual	
at the slots may not			nsions
exceed 244The maximum address		Mounting dimensions W×H×D (mm)	50×290×219
area of the interface		Slots required	2
(max. 2KB inputs /2 KB outputs) accumulated		Weight	approx. 0.72 kg
by 32 slaves may not		-	, Currents
be exceeded 2nd Interface	DP Slave Mode	Current consumption from S7-400 bus (5 VDC)	Typ. 1.0 A Max. 1.2 A
As for the 1st interface		Current consumption from	Total current consumption
	terface	the S7-400 bus (24 VDC) The CPU does not	of the components connected to the MPI/DP
Type of interface Insertable interface	Plug-in interface submodule IF-964-DP	consume any current at 24 V, and it only makes this	interfaces, with a maximum of 150 mA per interface
submodule		voltage available at the MPI/DP interface.	
Technical features as for the		Backup current	Τγρ 550 μΑ
	amming		Max. 1530 μA
Programming language	LAD, FBD, STL, SCL	maximum backup time	See manual Module
Instruction set	See instruction list		Specifications, chapter 3.3
	8	Incoming supply of external	5 VDC to 15 VDC
Bracket levels System functions (SFC)	See instruction list	backup voltage to the CPU	3 400 10 13 400

6.5 Technical Specifications of the CPU 416-2; (6ES7416-2XK04-0AB0, 6ES7416-2FK04-0AB0)

CPU and Version		Data Areas and Their Retentivity		
MLFB	6ES7416-2XK04-0AB0 6ES7416-2FK04-0AB0	Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)	
		Memory markers	16 Kbytes	
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update	 Retentivity can be set 	From MB 0 to MB 16383	
	emory	 Preset retentivity 	From MB 0 to MB 15	
Working memory		Clock memories	8 (1 memory byte)	
 Integrated 	1.4 Mbytes for code	Data blocks	Max. 4095 (DB 0 reserved)	
integrated	1.4 Mbytes for data	 Size 	Max. 64 Kbytes	
Load memory	1.1 mbytee for data	Local data (can be set)	Max. 32 Kbytes	
 Integrated 	256 Kbytes RAM	 Preset 	16 Kbytes	
Expandable FEPROM	With memory card (FLASH)		ocks	
	up to 64 Mbytes	OBs	See instruction list	
 Expandable RAM 	With memory card (RAM)	Size	Max. 64 Kbytes	
•	up to 64 Mbytes	Nesting depth	max. of haytoo	
Backup with battery	Yes, all data	 Per priority class 	24	
Typ. proc	essing times	Additionally in an error	2	
Processing times for		OB	-	
 Bit operations 	0.04 μs	FBs	Max. 2048	
 Word instructions 	0.04 μs	Size	Max. 64 Kbytes	
 Integer math 	0.04 µs	FCs	Max. 2048	
instructions		Size	Max. 64 Kbytes	
 Floating-point math instructions 	0.12 µs	Address Areas	(Inputs/Outputs)	
	and Their Retentivity	Total I/O address area	16 Kbytes/16 Kbytes	
S7 counters	2048	Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.	
 Retentivity can be set 	From Z 0 to Z 2047	MPI/DP interface	2 Kbytes/2 Kbytes	
 Preset 	From Z 0 to Z 7	DP interface	8 Kbytes/8 Kbytes	
 Counting range 	1 to 999	Process Image	16 Kbytes/16 Kbytes	
IEC counter	Yes		(can be set)	
 Type 	SFB	Preset	512 bytes/512 bytes	
S7 timers	2048	 Number of partial 	Max. 15	
 Retentivity can be set 	From T 0 to T 2047	process images		
 Preset 	No retentive timers	 Consistent data 	Max. 244 bytes	
Time range IEC timers	10 ms to 9990 s Yes	Digital channels	Max. 131072/ Max. 131072	
• Type	SFB	Of which central	Max. 131072/ Max. 131072	
		Analog channels	Max. 8192/ Max. 8192	
		Of which central	Max. 8192/ Max. 8192	

Configuration		S7 Message Functions		
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12	
Number of plug-in IMs (overall)	Max. 6	Symbol-related messages Number of messages 	Yes	
 IM 460 IM 463-2 	Max. 6 Max. 4	 Overall 100 ms grid 	Max. 1024 Max. 128	
Number of DP masters		- 500 ms grid - 1000 ms grid	Max. 512 Max. 1024	
IntegratedVia IM 467	2 Max. 4	Number of additional		
• Via CP 443-5 Extended IM 467 cannot be used with		 values per message With 100 ms grid With 500, 1000 ms 	Max. 1	
IM 467 cannot be used with mode	the CP 443-1 EX40 in PN IO	 With 500, 1000 ms grid Block-related messages 	Max. 10 Yes	
Number of plug-in S5 modules via adapter casing (in the central rack) Operable function modules and communication	Max. 6	Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200	
processors		ALARM_8 blocks	Yes	
• FM	Limited by the number of slots and the number of connections	Number of communication jobs for ALARM 8 blocks and	Max. 1800	
• CP 440	Limited by the number of slots	blocks for S7 communication (can be		
• CP 441	Limited by the number of connections	set) ● Preset	600	
 Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467 	Max. 14	Process control reports Number of archives that can log on simultaneously	Yes 32	
	ïme	(SFB 37 AR_SEND)		
Clock Buffered	Yes Yes		tup Functions	
 Resolution Accuracy at Power off 	1 ms Deviation per day 1.7 s	 Monitor/modify variable Variables 	Yes Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters	
 Power on Operating beurs counters 	Deviation per day 8.6 s	Number of variables	Max. 70	
 Operating hours counters Number 	8 0 to 7	Force	Yes	
NumberValue RangeGranularity	0 to 7 0 to 32767 hours 1 hour	Variables	Inputs/outputs, memory markers, distributed inputs/outputs	
Retentive	Yes	Number of variables	Max. 512	
Time synchronization	Yes	Status block	Yes	
 In PLC, on MPI and DP 		Single sequence	Yes	
		Diagnostic buffer	Yes	
		Number of entries	Max. 3200 (can be set)	
		Preset	120	
		Number of breakpoints	4	

Communicat	ion Functions	1st Interface D	P Master Mode
Programming device/OP	Yes	Utilities	
communication Number of connectable OPs	63 without message processing, 12 with message	 Programming device/OP communication 	Yes
	processing	– Routing	Yes
Number of connection	64, with one each of those	 S7 basic communication 	Yes
resources for S7	reserved for PG and OP	– S7 communication	Yes
connections via all interfaces and CPs		 – Onstant bus cycle 	Yes
Global data communication	Yes	time	103
Number of GD circuits	Max. 16	- SYNC/FREEZE	Yes
 Number of GD packages 		 Enable/disable DP slaves 	Yes
– Sender	Max. 16	Transmission rates	Up to 12 Mbps
 Receiver 	Max. 32	 Number of DP slaves 	Max. 32
 Size of GD packages 	Max. 64 bytes	Address area	Max. 2 Kbytes inputs/
 Of which consistent 	1 variable		2 Kbytes outputs
S7 basic communication	Yes	 User data per DP slave User data per DP slave 	Max. 244 bytes inputs, max.244 bytes outputs,
MPI Mode	via SFC X_SEND, X_RCV, X_GET and X_PUT	• User data per DF slave	max. 244 slots each with max. 128 bytes
DP Master Mode	via SFC I_GET and I_PUT	Note:	
 User data per job 	Max. 76 bytes	 Note: The accumulated 	
 Of which consistent 	1 variable	number of input bytes	
S7 communication	Yes	at the slots may not exceed 244	
 User data per job 	Max. 64 Kbytes	 The accumulated 	
 Of which consistent 	1 variable (462 bytes)	number of output bytes	
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)	at the slots may not exceed 244 • The maximum address	
 User data per job 	Max. 8 Kbytes	area of the interface	
 Of which consistent 		(max. 2KB inputs /2 KB	
Standard communication (FMS)	Yes (via CP and loadable FB)	outputs) accumulated by 32 slaves may not be exceeded	
Inter	faces	1st Interface D	DP Slave Mode
1st Int	terface	You can only configure the C	
Type of interface	Integrated	if the CPU has several interfa	aces.
Physical	RS 485/Profibus	Utilities	
Isolated	Yes	 Monitor/modify Programming 	Yes Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA	- Routing	Yes
Number of connection resources	MPI: 44 DP: 32, a diagnostic	DDB (GSD) file	http://www.ad.siemens.de/c si_e/gsd
	repeater in the segment reduces the number of	Transmission rate	Up to 12 Mbps
	connection resources by 1	Intermediate memory	244 bytes inputs/ 244 bytes outputs
Functi	onality	 virtual slots 	Max. 32
• MPI	Yes	 User data per 	Max. 32 bytes
PROFIBUS DP	DP master/DP slave	address area	-
	e MPI Mode	 Of which consistent 	*
Utilities		-	terface
 Programming device/OP 	Yes	Type of interface	Integrated
communication		Physical	RS 485/Profibus
 Routing 	Yes	Isolated	Yes Max 150 mA
 Global data communication 	Yes	Power supply to interface (15 VDC to 30 VDC) Number of connection	Max. 150 mA
 S7 basic communication 	Yes	resources	32, a diagnostic repeater on the segment reduces the number of connection
 S7 communication 	Yes		resources by 1
 Transmission rates 	Up to 12 Mbps		

	Functionality		CiR synchronization time	
•	PROFIBUS DP	DP Master/DP Slave	Base load	100 ms
	2nd Interface D	P Master Mode	Time per I/O byte	40 µs
•	Utilities		Clock sy	nchronism
	 Programming device/OP 	Yes	User data per clock synchronous slave	Max. 244 bytes
	communication Routing 	Yes	Maximum number of bytes and slaves in a process	The following applies: Number of bytes/100 +
	 S7 basic communication 	Yes	image partition Constant bus cycle time	number of slaves <40 Yes
	 S7 communication 	Yes	Shortest clock pulse	1 ms
	 Constant bus cycle time 	Yes	Longest pulse clock see manual <i>Clock</i>	0.5 ms without use of SFC 126, 127
	– SYNC/FREEZE	Yes	Synchronism	
	 Enable/disable DP slaves 	Yes	Dime Mounting dimensions	nsions 25×290×219
•	Transmission rates	Up to 12 Mbps	W×H×D (mm)	
•	Number of DP slaves	Max. 125	Slots required	1
•	Address area	Max. 8 Kbytes inputs/ 8	Weight	approx. 0.72 kg
		Kbytes outputs		, Currents
•	User data per DP slave	Max. 244 bytes inputs / 244 bytes outputs distributed over 244 slots	Current consumption from S7-400 bus (5 VDC)	Тур. 1.0 А Мах. 1.2 А
	2nd Interface I	each with 128 bytes	the S7-400 bus (24 VDC) of t The CPU does not con consume any current at inte	Total current consumption of the components
٨٥	for the 1st interface			connected to the MPI/DP interfaces, with a maximum
AS		mming		of 150 mA per interface
Dro	ogramming language	LAD, FBD, STL, SCL	voltage available at the	
	struction set	See instruction list	MPI/DP interface.	
	acket levels	8	Backup current	Typ. 550 μA
	stem functions (SFC)	See instruction list		Max. 1539 µA
Nu	mber of SFCs active at		maximum backup time	See manual <i>Module</i> <i>Specifications</i> , chapter 3.3
	e same time for every and		Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
•	DP_SYC_FR	2	Power loss	Typ. 4.5 W
•	D_ACT_DP	4		
•	RD_REC	8		
•	WR_REC	8		
•	WR_PARM	8		
•	PARM_MOD	1		
•	WR_DPARM	2		
•	_ DPNRM_DG	8		
•	RDSYSST	1 to 8		
•	DP_TOPOL	1		
		See instruction list		
	mber of SFBs active at same time			
•	RD_REC	8		
•	WR_REC	8		
Us	er program protection	Password protection		
Ac	cess to consistent data the process image	Yes		

Technical Specifications of the CPU 416-3; 6.6 (6ES7416-3XL04-0AB0)

CPU and Version		Data Areas and	Their Retentivity	
MLFB	6ES7416-3XL04-0AB0	Total retentive data area	Total working and load	
Firmware version		(incl. memory markers, timers, counters)	memory (with backup battery)	
Associated programming package	As of STEP 7 5.2 SP1 HF3 with HW-Update	Memory markers	16 Kbytes	
	mory	Retentivity can be set	From MB 0 to MB 16383	
Working memory		Preset retentivity	From MB 0 to MB 15	
 Integrated 	2.8 Mbytes for code	Clock memories	8 (1 memory byte)	
	2.8 Mbytes for data	Data blocks	Max. 4095 (DB 0 reserved)	
Load memory		Size	Max. 64 Kbytes	
 Integrated 	256 Kbytes RAM	Local data (can be set)	Max. 32 Kbytes	
 Expandable FEPROM 	With memory card (FLASH)	Preset	16 Kbytes	
	up to 64 Mbytes	Bl	ocks	
 Expandable RAM 	With memory card (RAM)	OBs	See instruction list	
	up to 64 Mbytes	Size	Max. 64 Kbytes	
Backup with battery	Yes, all data	Nesting depth		
	essing Times	 Per priority class 	24	
Processing times for		Additionally in an error	2	
 Bit operations 	0.04 μs	OB		
 Word instructions 	0.04 μs	FBs	Max. 2048	
 Integer math 	0.04 μs	Size	Max. 64 Kbytes	
instructions	0.40	FCs	Max. 2048	
 Floating-point math instructions 	0.12µs	Size	Max. 64 Kbytes	
	and Their Retentivity	Address Areas (Inputs/Outputs)		
S7 counters	2048	Total I/O address area	16 Kbytes/16 Kbytes	
Retentivity can be set	From Z 0 to Z 2047	Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.	
 Preset 	From Z 0 to Z 7	MPI/DP interface	2 Kbytes/2 Kbytes	
 Counting range 	1 to 999	DP interface	8 Kbytes/8 Kbytes	
IEC counter	Yes	Process Image	16 Kbytes/16 Kbytes	
 Type 	SFB		(can be set)	
S7 timers	2048	Preset	512 bytes/512 bytes	
 Retentivity can be set 	From T 0 to T 2047	 Number of process 	Max. 15	
 Preset 	No retentive timers	images partitions	May 044 hidaa	
 Time range 	10 ms to 9990 s	Consistent data	Max. 244 bytes	
IEC timers	Yes SFB	Digital channels	Max. 131072/ Max. 131072	
• Type		Of which central	Max. 131072/ Max. 131072	
		Analog channels	Max. 8192/ Max. 8192	
		Of which central	Max. 8192/ Max. 8192	

Configuration		S7 Message Functions		
Central racks/expansion units	Max. 1/21	Number of stations that can log on for message functions (e.g. WIN CC or	Max. 12	
Multicomputing	Max. 4 CPUs (with UR1 or UR2)	SIMATIC OP)		
Number of plug-in IMs (overall)	Max. 6	Symbol-related messagesNumber of messages	Yes	
• IM 460	Max. 6	– Overall	Max. 1024	
 IM 460 IM 463-2 	Max. 6 Max. 4	– 100 ms grid	Max. 128	
Number of DP masters	Max. 4	– 500 ms grid	Max. 512	
	0	- 1000 ms grid	Max. 1024	
integrated	2	Number of additional		
	1	values per message		
• Via IM 467	Max. 4	 With 100 ms grid 	Max. 1	
 Via CP 443-5 Extended IM 467 cannot be used with 		 With 500, 1000 ms grid 	Max. 10	
IM 467 cannot be used with	the CP 443-1 EX40 in PN IO	Block-related messages	Yes	
mode Number of plug-in S5 modules via adapter casing	Max. 6	Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ	Max. 200	
(in the central rack)		blocks		
Operable function modules		ALARM 8 blocks	Yes	
and communication		Number of	Max. 1800	
ProcessorsFM	Limited by the number of slots and the number of connections	communication jobs for ALARM_8 blocks and blocks for S7 communication (can be		
• CP 440	Limited by the number of slots	set)		
• CP 441	Limited by the number of connections	Preset Process control reports Number of archives that	600 Yes 32	
• Profibus and Ethernet CPs incl. CP 443-5	Max. 14	can log on simultaneously (SFB 37 AR_SEND)	52	
Extended and IM 467		-	tup Functions	
1	ïme	Monitor/modify variable	Yes	
ClockBuffered	Yes Yes	Variables	Inputs/outputs, memory markers, DB, distributed	
Resolution	1 ms		inputs/outputs, timers,	
 Accuracy at 			counters	
 Accuracy at Power off 	Deviation per day 1.7 s	Number of variables	Max. 70	
 Power on 	Deviation per day 8.6 s	Force Variables	Yes	
Runtime meter	8	Variables	Inputs/outputs, memory markers, distributed inputs/outputs	
Number	0 to 7	Number of variables	Max. 512	
 Value Range 	0 to 32767 hours	Status block	Yes	
 Granularity 	1 hour	Single sequence	Yes	
Retentive	Yes	Diagnostic buffer	Yes	
Time synchronization	Yes	Number of entries	Max. 3200 (can be set)	
 In PLC, on MPI, DP and IF 964 DP 	as master or slave	Preset Number of breakpoints	120 4	

	ion Functions		e DP Master Mode
Programming device/OP communication	Yes	 Utilities Programming 	Yes
Number of connectable	63 without message	 Programming device/OP 	100
OPs	processing,	communication	
0.0	12 with message		Vee
	processing	- Routing	Yes
Number of connection	64, with one each of those	 S7 basic 	Yes
resources for S7	reserved for PG and OP	communication	X
connections via all		 S7 communication 	
interfaces and CPs		 Constant bus cyc 	e Yes
Global data communication	Yes	time	
 Number of GD circuits 	Max. 16	– SYNC/FREEZE	Yes
 Number of GD packages 		 Enable/disable DI slaves 	P Yes
 Sender 	Max. 16	 Transmission rates 	Up to 12 Mbps
 Receiver 	Max. 32	Number of DP slaves	Max. 32
Size of GD packages	Max. 64 bytes	Address area	Max. 2 Kbytes inputs/2
 Of which consistent 	1 variable		Kbytes outputs
S7 basic communication	Yes	User data per DP slav	
MPI Mode	via SFC X SEND, X RCV,	User data per DP slav	max.244 bytes outputs,
	X_GET and X_PUT		max. 244 slots each with max. 128 bytes
DP Master Mode	via SFC I_GET and I_PUT	 .	
User data per job	Max. 76 bytes	Note:	
 Of which consistent 	1 variable	The accumulated	
S7 communication	Yes	number of input bytes at the slots may not	
 User data per job 	Max. 64 Kbytes	exceed 244	
 Of which consistent 	1 variable (462 bytes)	 The accumulated 	
S5-compatible communication	via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)	number of output byte at the slots may not exceed 244	S
 User data per job 	Max. 8 Kbytes	The maximum addres	e
 Of which consistent 	240 bytes	area of the interface	5
Standard communication	Yes (via CP and loadable	(max. 2KB inputs /2 K	В
(FMS)	FB)	outputs) accumulated	
Inter	faces	by 32 slaves may not be exceeded	
	erface		e DP Slave Mode
Type of interface	Integrated		
Physical	RS 485/Profibus	if the CPU has several int	e CPU once as a DP slave even
Isolated	Yes	 Utilities 	
Power supply to interface	Max. 150 mA		Vee
(15 VDC to 30 VDC)		– Monitor/modify	Yes
Number of connection	MPI: 44	 Programming 	Yes
resources	DP: 32 a diagnostic	 Routing 	Yes
	repeater in the strand	• DDB (GSD) file	http://www.ad.siemens.de/o
	reduces the number of		si_e/gsd
	connection resources by 1	Transmission rate	Up to 12 Mbps
	onality	Intermediate memory	244 bytes inputs/ 244 bytes
• MPI	Yes		inputs
 PROFIBUS DP 	DP master/DP slave	 virtual slots 	Max. 32
1st Interfac	e MPI Mode	 User data per 	Max. 32 bytes
Utilities		address area	
 Programming device/OP communication 	Yes	 Of which consister 	nt 32 bytes
	Vee		
 Routing Clabel data 	Yes		
 Global data communication 	Yes		
 S7 basic communication 	Yes		
_			
 S7 communication Transmission rates 	Yes Up to 12 Mbps		

Transmission rates
 Up to 12 Mbps

	2nd In	iterface	Number of SFCs active at	
Тур	e of interface	Integrated	the same time for every	
Phy	vsical	RS 485/Profibus	strand	
Isol	ated	Yes	 DPSYC_FR 	2
Pov	ver supply to interface	Max. 150 mA	D_ACT_DP	4
	VDC to 30 VDC)		RD_REC	8
	mber of connection	32, a diagnostic repeater in	• WR_REC	8
reso	ources	the strand reduces the	• WR_PARM	8
		number of connection resources by 1	 PARM_MOD 	1
	Funct	ionality	WR_DPARM	2
•	PROFIBUS DP	DP master/DP slave	 DPNRM_DG 	8
-		DP Master Mode	RDSYSST	1 to 8
•	Utilities		DP_TOPOL	1
	 Programming 	Yes	System function blocks (SFB)	See instruction list
	device/OP communication		Number of SFBs active at the same time	
	 Routing 	Yes	RD REC	8
	 S7 basic 	Yes	WR REC	8
	communication		User program protection	Password protection
	 S7 communication 	Yes	Access to consistent data	Yes
	 Constant bus cycle 	Yes	in the process image	
	time	No.	CiR synchro	onization time
	 SYNC/FREEZE Enable/disable DP 	Yes	Base load	100 ms
	 Enable/disable DP slaves 	Yes	Time per I/O byte	40 µs
•	Transmission rates	Up to 12 Mbps	Clock sy	nchronism
	Number of DP slaves	Max. 125	User data per clock	Max. 244 bytes
	Address area	Max. 8 Kbytes inputs/ 8	synchronous slave	T ()
		Kbytes outputs	Maximum number of bytes and slaves in a process	The following applies:
	User data per DP slave User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs,	image partition	NUmber of bytes/50 + number of slaves
•	User data per Dr slave	max. 244 slots each with	Constant bus cycle time	Yes
		max. 128 bytes	Shortest clock pulse	1 ms
			Longest clock pulse	0.5 ms without use of SFC
	Note:		see manual Clock Synchronism	126, 127
	The accumulated number of input bytes		-	nsions
	at the slots may not		Mounting dimensions	50×290×219
•	exceed 244		W×H×D (mm)	
•	The accumulated number of output bytes		Slots required	2
	at the slots may not		Weight	approx. 1.07 kg
	exceed 244		•	, Currents
•	The maximum address		Current consumption from S7-400 bus (5 VDC)	Typ. 1.2 A
	area of the interface (max. 2KB inputs /2 KB		. ,	Max. 1.4 A
	outputs) accumulated		Current consumption from the S7-400 bus (24 VDC)	Total current consumption of the components
	by 32 slaves may not		The CPU does not	connected to the MPI/DP
	be exceeded		consume any current at 24	interfaces, with a maximum
Δe f	2nd Interface	DP Slave Mode	V, and it only makes this voltage available at the	of 150 mA per interface
7.91		terface	MPI/DP interface.	_
Tvn	e of interface	Plug-in interface submodule	Backup current	Typ. 550 μA
	ertable interface	IF-964-DP		Max. 1530 μA
	module		maximum backup time	See manual <i>Module</i>
	hnical features as for the		Incoming supply of external	<i>Specifications</i> , chapter 3.3 5 VDC to 15 VDC
	v	amming	backup voltage to the CPU	
	gramming language	LAD, FBD, STL, SCL	Power loss	Typ. 5.0 W
	ruction set	See instruction list		
Bra	cket levels	8		
-	tem functions (SFC)	See instruction list		

6.7 Technical Specifications of the CPU 417-4; (6ES7417-4XL04-0AB0)

CPU and Version			
MLFB	6ES7417-4XL04-0AB0		
Firmware version	V 1.0		
Associated programming	As of STEP 7 5.2 SP1 HF3		
package	with HW-Update		
Mei	nory		
Working memory			
 Integrated 	10 Mbytes for code		
	10 Mbytes for data		
Load memory			
 Integrated 	256 Kbytes RAM		
Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes		
Expandable RAM	With memory card (RAM)		
	up to 64 Mbytes		
Backup with battery	Yes, all data		
Process	ing Times		
Processing times for			
Bit operations	0.03 µs		
Word instructions	0.03 µs		
 Integer math instructions 	0.03 µs		
 Floating-point math instructions 	0.09 µs		
Timers/Counters a	nd Their Retentivity		
S7 counters	2048		
Retentivity can be set	From Z 0 to Z 2047		
Preset	From Z 0 to Z 7		
Counting range	1 to 999		
IEC counter	Yes		
• Type	SFB		
S7 timers	2048		
Retentivity can be set	From T 0 to T 2047		
Preset	No retentive timers		
Time range	10 ms to 9990 s		
IEC timers	Yes		
• Туре	SFB		
	Their Retentivity		
Total retentive data areas	Total working and load		
(including memory bits; times; counts)	memory (with backup battery)		
Memory markers	16 Kbytes		
Retentivity can be set	From MB 0 to MB 16383		
Preset retentivity	From MB 0 to MB 15		
Clock memories	8 (1 memory byte)		
Data blocks	Max. 8191 (DB 0 reserved)		
Size	Max. 64 Kbytes		
Local data (can be set)	Max. 64 Kbytes		
Preset	32 Kbytes		
<u>L</u>			

Blo	ocks
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
 Per priority class 	24
 Additionally in an error OB 	2
FBs	Max. 6144
Size	Max. 64 Kbytes
FCs	Max. 6144
• Size	Max. 64 Kbytes
Address Areas	(Inputs/Outputs)
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	incl. diagnostics addresses for I/O interfaces, etc.
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
Process Image	16 Kbytes/16 Kbytes (can be set)
Preset	1024 bytes/1024 bytes
 Number of partial process images 	Max. 15
 Consistent data 	Max. 244 bytes
Digital channels	Max. 131072/ Max. 131072
Of which central	Max. 131072/ Max. 131072
Analog channels	Max. 8192/ Max. 8192
Of which central	Max. 8192/ Max. 8192

Configuration		S7 Message Functions		
Central racks/expansion units Multicomputing	Max. 1/21 Max. 4 CPUs (with UR1 or UR2)	Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 16	
Number of plug-in IMs (overall)	Max. 6	Symbol-related messages Number of messages 	Yes	
• IM 460	Mox 6	– Overall	Max. 1024	
	Max. 6		Max. 128	
 IM 463-2 	Max. 4	 100 ms grid 	Max. 512	
Number of DP masters	0	 – 500 ms grid 	Max. 1024	
Integrated	2	 1000 ms grid 		
• Via IF 964-DP	2	 Number of additional 		
• Via IM 467	Max. 4	values per message		
 Via CP 443-5 Extended 		 With 100 ms grid 	Max. 1	
	the CP 443-5 Extended the CP 443–1 EX40 in PN IO	 With 500, 1000 ms grid 	Max. 10	
mode		Block-related messages	Yes	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6	 Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ 	Max. 200	
Operable function modules and communication		blocks		
processors		ALARM_8 blocks	Yes	
• FM	Limited by the number of slots and the number of connections	 Number of communication jobs for ALARM_8 blocks and blocks for S7 	Max. 10000	
• CP 440	Limited by the number of slots	communication (can be set)		
• CP 441	Limited by the number of connections	Preset Process control reports	1200 Yes	
 Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467 	Max. 14	Number of archives that can log on simultaneously (SFB 37 AR_SEND)	64	
	Yes	Test and Star	tup Functions	
Clock Buffered	Yes	Monitor/modify variable	Yes	
ResolutionAccuracy at	1 ms	Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters	
 Power off 	Deviation per day 1.7 s	 Number of variables 	Max. 70	
– Power on	Deviation per day 8.6 s	Force	Yes	
Runtime meter	8	Variables	Inputs/outputs, memory	
Number	0 to 7		markers, distributed	
Value Range	0 to 32767 hours		inputs/outputs	
Granularity	1 hour	Number of variables	Max. 512	
Retentive	Yes	Status block	Yes	
Time synchronization	Yes	Single sequence	Yes	
 In PLC, on MPI, DP and IF 964 DP 	as master or slave	Diagnostic buffer Number of entries 	Yes Max. 3200 (can be set)	
		 Preset Number of breakpoints 	120 4	

X_GET and X_PUTDP Master Modexx_GET and X_PUTmax. 244 slots each max. 128 bytes• DP Master Modevia SFC I_GET and I_PUTMax. 76 bytesmax. 128 bytes- Of which consistent1 variableYesNote:• User data per jobMax. 64 KbytesThe accumulated number of input bytes at the slots may not exceed 244The accumulated number of output bytes at the slots may not exceed 244• User data per jobMax. 8 Kbytes- Of which consistent1 variable (462 bytes)• User data per jobMax. 8 Kbytes- Of which consistent240 bytes• User data per jobMax. 8 Kbytes- Of which consistent240 bytesYes (via CP and loadable FB)Yes (via CP and loadable FB)InterfacesYes (via CP and loadable FB)InterfaceTst Interface OP Slave ModeType of interfaceInterfaceType of interfaceInterfacePower supply to interface (15 VDC to 30 VDC)MPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1Number of connection resourcesMPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1EurctionalityTransmission rateUp to 12 Mbps		on Functions	Transmission rates	Up to 12 Mbps
Number of connectable 63 without message processing, 16 with message processing - Programming device/OP Yes Number of connection 64, with one each of those reserved for PG and OP - Routing Yes Of which consistent Yes - S7 basic Yes Of which consistent Yes - Constant bus cycle Yes - Strongenication Yes - Constant bus cycle Yes - Strongenication Yes - Constant bus cycle Yes - Strongenication Yes - Constant bus cycle Yes - MPI Mode wax. 32 Number of DP slaves Max. 2 Kotytes inputs Stroe of Chine consistent 1 variable Yes - Griwhich consistent 1 variable Stroemputible via SFC X SEND, X RCV, X GET and X PUT User data per DP slave Max. 2 Kotytes inputs - Of which consistent 1 variable Yes - Transmission rates Up to 12 Mbps Standard communication Yes - Of which consistent 1 variable - Max. 32 Yes - Of which consistent 1 variable - Max. 4 Kotytes - Of which consistent 1 variable - Max. 32		Yes	1st Interface D	P Master Mode
DPs processing fb fb 16 with message processing fb fb Number of connaction 64, with one sach of those resources and CPs Fb Fb Clobal data communication Yes ST Zommunication Yes - Sender Max. 16 - Fc Constant bus cycle time Yes - Sender Max. 16 - Fc Status communication Yes - Steeciver Max. 32 Transmission rates Up to 12 Mbps 5 basic communication Yes Status communication Yes 5 basic communication Yes Max. 76 bytes Max. 24 bytes input Kbytes outputs - Of which consistent 1 variable Yes Max. 76 bytes - Of which consistent 1 variable Yes Max. 76 bytes - Of which consistent 1 variable Yes Max. 76 bytes - Of which consistent 1 variable Yes Max. 76 bytes - Of which consistent 1 variable Yes Max. 76 variable - Of which consistent 1 variable Yes The accumulated number of input bytes at the isots may not exceed 244 - The accumulated number of conputs the CPU noe as a DP slave Note: 1 St Interface Integrated	communication		Utilities	
Number of connection 64, with one each of those resources for S7 resources for S7 resources for S7 – Houling Yes Communication Yes – ST basic Yes Number of GD Max. 16 – ST basic Yes Number of GD circuits Max. 16 – ST Number of GD Yes - Sender Max. 16 – St NAC/FREZZ Yes - Of which consistent 1 variable Strace of GD packages Max. 24 bytes inputs Stace of GD packages Vas. 76 bytes – Of which consistent Yes - Of which consistent Yes User data per JD Max. 76 bytes – User data per jD Max. 64 kbytes - Of which consistent Yes – User data per jD Max. 76 bytes - Of which consistent Yes (Vac CP ad-1 or 43-5) Note: The accumulated number of oluput bytes at the slots may not exceed 244 The maximum address area of the interface Type of interface The accumulated the interface integrated Type of interface Programming Yes – Programming Yes – Programming Yes - Programming Yes – Of which consistent Yes		processing, 16 with message	device/OP	Yes
resources for S7 ormunication reserved for PG and OP communication S7 communication S7 communication S8 cord GD packages - Sender - Receiver - Receiver - Receiver - Receiver - Receiver - Of which consistent - Neter - Of which consistent - Of which consistent - Neter - Of which consistent - Neter - Of which consistent - Neter - Ne			 Routing 	Yes
 Mumber of GD circuits Number of GD circuits Max. 16 Number of GD circuits Max. 16 Number of GD circuits Max. 16 Stee of GD packages Size of GD packages Max. 32 Size of GD packages Max. 64 bytes Of which consistent Ves MPI Mode Va SFC LSEND, X, RCV, X, GET and L, PUT User data per job Max. 76 bytes Of which consistent Ves via SFC LSEND, X, RCV, X, GET and X, PUT User data per job Max. 76 bytes Max. 76 bytes Max. 76 bytes Max. 76 bytes User data per job Max. 76 bytes Max. 76 bytes Max. 76 bytes User data per job Max. 76 bytes Max. 84 Koytes Of which consistent Ves (via SPC LGEC) max. via 10 CP 443-1 or 443-5) Wase data per job Max. 8 Koytes Of which consistent Ves (via CP and loadable FB) User data per job Max. 8 Koytes Of which consistent Ves (via CP and loadable FB) Interface Transmission rate Vou can ony configure the CPU once as a DP slaw if the CPU has several interfaces. Utilities ODB (GSD) file MPI-K4 Proogramming Yes Oper communication Proogramming Yes Of which consistent	resources for S7 connections via all		communication	
Number of GD circuits Max. 16 Number of GD packages Max. 16 - Sender Max. 32 Size of GD packages Max. 64 bytes - Of which consistent 1 variable S7 basic communication Yes MPI Mode via SFC X_SEND, X_RCV, X_GET and X_PUT User data per job Max. 76 bytes - Of which consistent 1 variable S7 communication Yes - User data per job Max. 64 Kbytes - Of which consistent 1 variable (462 bytes) S-compatible via FC AG, SEND and communication Ves (via CP and loadable FB) Ves (via CP and loadable FB) User data per job Max 8 Kbytes - Of which consistent Yes (via CP and loadable FB) (FMS) Interface Type of interface Integrated Yes Yes (via CP and loadable FB) Power supply to interface Max 150 mA Transmission rate Up to 12 Mbps Itherface Programming Yes - Routing PROFIBUS DP Preaster/ DP master/	interfaces and CPs			
 Number of GD packages Size of GD packages Of which consistent Variable Size of GD packages Max. 16 Receiver Max. 22 Size of GD packages Max. 46 bytes Of which consistent Yes MPI Mode Yes Address area User data per iob Max. 76 bytes Of which consistent Yes User data per iob Max. 76 bytes Of which consistent Yes User data per iob Max. 76 bytes Of which consistent Yes User data per iob Max. 76 bytes Of which consistent Yes User data per iob Max. 76 bytes Of which consistent Yes (via CP and loadable The accumulated number of output bytes at the siots may not exceed 244 The accumulated number of output bytes at the siots may not exceed 244 The accumulated number of output bytes at the siots may not exceed 244 The accumulated mumber of output bytes at the siots may not exceed 244 Extinterface FB) User data per iob Max. 8 (bytes FB) Integrated FB) MPI 44 Solated PROFIBUS DP Programming Yes PROFIBUS DP Programming Yes PROFIBUS DP Programming Yes Programming Yes via SFC X_SEND, communication Proparaming Yes via SFC X SEND, communication Proparating Yes via SFC X_S				res
 Number of GD packages Sender Max. 16 Receiver Max. 32 Size of GD packages Max. 64 bytes Of which consistent 1 variable Statisc communication Yes MPI Mode Via SFC X SEND, X, RCV, X, GET and X, PUT DP Master Mode Via SFC X SEND, X, RCV, X, GET and X, PUT User data per job Max. 76 bytes Of which consistent 1 variable Stormunication Yes User data per job Max. 76 bytes Of which consistent 1 variable (462 bytes) User data per job Max. 76 bytes Of which consistent 1 variable (462 bytes) User data per job Max. 84 bytes Of which consistent 1 variable (462 bytes) Stormunication XG RECV, max. via 10 CP 443-1 or 443-50 User data per job Max. 84 bytes Of which consistent 240 bytes User data per job Max. 84 bytes Of which consistent 1240 bytes User data per job Max. 84 bytes Of which consistent 240 bytes User data per job Max. 84 bytes Of which consistent 1420 bytes User data per job Max. 84 bytes Tat Interface DP Slave Mode You can only configure the CPU once as a DP slave if the CPU has several interfaces. Programming Yes PROFIBUS DP DP master/DP slave Interface MPI Mode Interface MPI Mode Interface MPI Mode Interface IP /li>		Max. 16		Yes
 Sender Max. 16 Receiver Max. 32 Size of GD packages Max. 64 bytes Of which consistent 1 variable Transmission rates Variable Number of DP slaves Address area Max. 24 bytes inputs Kbytes outputs User data per job Max. 76 bytes Of which consistent 1 variable Variable (42 bytes) User data per job Max. 64 Kbytes Of which consistent 1 variable (42 bytes) User data per job Max. 64 Kbytes Of which consistent 1 variable (42 bytes) User data per job Max. 84 Kbytes Of which consistent 240 bytes Yas Grad Cormunication FB User data per job Max 845/Profibus Standard communication KPI: 44 The accumulated interface The maximum address area of the interface frace (max. 2KB inputs / 2 KB outputs) accumulated by 32 slaves may not be exceed 244 The maximum address area of the interface DP Slave Mode Vou can only configure the CPU once as a DP slav if the CPU has several interface. Willities Programming Yes outputs address area Of which consistent 32 bytes Transmission rate Up to 12 Mbps Transmission rate Up to 12 Mbps Transmission rate Up to 12 Mbps Transmission rate Ves inputs 24 bytes inputs / 24 bytes inputs / 24 bytes inputs / 24 bytes / 24 bytes inputs / 24 bytes / 24 by	packages		– Enable/disable DP	
 Number of DP slaves Address area Max. 32 Address area Max. 2 (Stytes input rax. 244 sytes output max. 244 sytes output max. 244 bytes output max. 244 bytes output max. 244 bytes output max. 244 bytes output max. 245 bytes The accumulated numer of output bytes at the slots may not exceed 244 The accumulated number of input bytes at the slots may not exceed 244 The accumulated numer address area of the interface The accumulated The	– Sender	Max. 16		Lin to 12 Mbns
 Size of GD packages Max. 64 bytes Of which consistent 1 variable S7 basic communication MPI Mode Ves Max. 2 Kbytes inputs User data per job Max. 76 bytes Of which consistent 1 variable S7 communication Ves User data per job Max. 76 bytes Of which consistent 1 variable S7 communication Ves User data per job Max. 76 bytes Of which consistent 1 variable S7 communication Ves User data per job Max. 64 Kbytes Of which consistent 1 variable Kett and X, PUT Was CA GA (SEND and Communication CP 443-10 variable FB User data per job Max. 8 Kbytes Of which consistent 240 bytes Standard communication Yes (via CP and loadable FB) Interfaces The functionality MPI Yes PROFIBUS DP PROFORMING Yes PROFIBUS DP PROFIBUS DP PROFIBUS DP PROFORMING Yes PROFIBUS DP PROFORMING Yes PROFIBUS DP PROFORMING Yes (Vas CA SEND, X, CVE, GET and Communication Stalated Yes Programming Yes Global data Yes Communication Yes via SFC X, SEND, communication S Tasic Yes via SFC X, SEND, communication S Tasic Yes via SFC X, SEND, communication S Tasic Yes via SFC X,	 Receiver 	Max. 32		
- Of which consistent 1 variable Yes via SFC X_SEND, X_RCV, X_GET and X_PUT User data per job Max. 76 bytes - Of which consistent 1 variable Yes Yes User data per job Max. 76 bytes - Of which consistent 1 variable Yes Max. 76 bytes - Of which consistent 1 variable Yes Max. 84 Kbytes - Of which consistent 1 variable (462 bytes) Standard communication XG RECV, max. via 10 CP443-1 or 443-5) Max. 8 Kbytes - Of which consistent 240 bytes Yes (via CP and loadable FMs) Yes (via CP and loadable FMs) FMS) FB Interfaces Note: Standard communication MS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA Physical MS 485/Profibus Isolated Pis 22 a diagnostic repeater in the strand reduces the number of connection resources by 1 Ist Interface MPI Mode Ist Interface MPI Mode Vitilities - Of which consistent 32 bytes - Of which con	 Size of GD packages 	Max. 64 bytes		
37 basic communication Yes MPI Mode via SFC X_SEND, X_RCV, X_GET and X_PUT DP Master Mode via SFC I_GET and I_PUT User data per job Max. 76 bytes - Of which consistent 1 variable (462 bytes) Sc-compatible via FC AG SEND and communication Sc-compatible via FC AG SEND and communication CF 443-1 or 443-5) Max. 64 kbytes - Of which consistent 1 variable (462 bytes) Sc-compatible via FC AG SEND and communication CF 443-1 or 443-5) Max. 8 kbytes - Of which consistent 240 bytes Yes (via CP and loadable FB) FB) Interfaces Yes (via CP and loadable FB) FMysical RS 485/Profibus Isolated Yes Proyer of interface MR: 43 10 mA Physical RS 485/Profibus Isolated Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode Visc inputs/2 Kes Willities - Of which consistent 32 bytes - Programming device/OP communication Yes PROFIBUS DP DP master/DP slave	 Of which consistent 	1 variable	 Address area 	
 MPI Mode via SFC X_SEND, X_RCV, X_GET and X_PUT max. 244 bytes output max. 244 bytes Of which consistent 1 variable (462 bytes) Socompatible via FC A (S SEND and A G RECV, max. via 10 CP 443-1 or 443-5) User data per job Max. 8 bytes Of which consistent 240 bytes Standard communication FB) Interface FB) Interface Integrated FPs Solated Yes Proyer of interface Integrated Prevision of connection mesources by 1 Functionality MPI Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode Utilities PROFIBUS DP DP master/DP slave Interface MPI Mode Utilities Programming Yes address area Programming Yes address area Of which consistent Yes (max. 150 mA MPI Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode Utilities Of which consistent Yes (max. 24 bytes inputs/24- outputs) Interface MPI Mode Utilities Of which consistent Yes (max. 32 bytes address area Of which consistent Yes (max. 120 mA (15 VDC to 30 VDC) 	S7 basic communication	Yes	 User data per DP slave 	, ,
User data per job Max. 76 bytes - Of which consistent 1 variable 37 communication Yes User data per job Max. 64 Kbytes - Of which consistent 1 variable (462 bytes) 55-compatible via FC AG_SEND and AG_RECV, max. via 10 CP 443-15 or 443-5) • User data per job Max. 8 Kbytes - Of which consistent 240 bytes Standard communication Yes (via CP and loadable FB) FMS) Interface FMS) Interface Prop of interface Integrated Prysical RS 485/Profibus solated Yes Over supply to interface Max. 150 mA 15 VDC to 30 VDC) MPI: 44 DFROFIBUS DP DP master/DP slave Itilities - Of which consistent - Programming device/OP communication Yes - Routing Yes Of shick face - Routing Yes Of which consistent - Routing Yes Of which consistent - Stasic communication Yes via SFC X_SEND, communication - Stasic communication Yes via SFC X_SEND, communi	MPI Mode		-	max. 244 bytes outputs, max. 244 slots each with
 Of which consistent 1 variable S7 communication Yes User data per job Max. 64 Kbytes Of which consistent 1 variable (462 bytes) via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5) User data per job Max. 8 Kbytes Of which consistent 240 bytes Yes (via CP and loadable FB) Interfaces Yes (via CP and loadable FB) Interface Interface The maximum address area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not exceed 244 The accumulated number of output bytes area of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Vau can only configure the CPU once as a DP slave if the CPU and as a dofteres area interface. Utilities PROFIBUS DP DP master/DP slave Virtual slots Max. 32 bytes address area - Of which consistent 32 bytes isolated Yes (CMP communication - Routing Yes (CMP communication - ST basic Communication - ST basic Communication - ST basic Communication	 DP Master Mode 	via SFC I_GET and I_PUT		max. 128 bytes
 Of which consistent 1 variable S7 communication Ves User data per job Max. 64 Kbytes Of which consistent 1 variable (462 bytes) S5-compatible via FC AG_SEND and AG_RECV_max. via 10 CP 443-1 or 443-5) User data per job Max. 8 Kbytes Of which consistent 240 bytes Standard communication Yes (via CP and loadable FB) Interfaces Yes (via CP and loadable FB) Interface The accumulated number of output bytes area of the interface (max. 2KB inputs / 2KB outputs) accumulated by 32 slaves may not be exceeded St Interface The maximum address area of the interface (max. 150 mA St VDC to 30 VDC) MPI Yes PROFIBUS DP Utilities Programming Yes Interface MPI Mode Utilities Programming Yes Of which consistent 32 bytes Solated Yes Of which consistent 32 bytes 	 User data per job 	Max. 76 bytes	.	
27 communication Yes User data per job Max. 64 Kbytes - Of which consistent 1 variable (462 bytes) yia FC AG_SEND and CP 443-1 or 443-5) CP 443-1 or 443-5) The accumulated User data per job Max. 8 Kbytes - Of which consistent 240 bytes Yes (via CP and loadable FB) Interfaces FB) Interface FB) Interface Interface Yes (via CP and loadable FB) Interfaces FB) Ower supply to interface Integrated Yes Yes Yes for connection MPI: 44 Solated Yes Ower supply to interface Max. 150 mA (15 VDC to 30 VDC) MPI Vumber of connection resources by 1 MPI Functionality MPI MPI Yes PROFIBUS DP DP master/DP slave It litterface MPI Mode Isa data Yes Of which consistent 32 bytes - Of which consistent 32 bytes - Programming Yes Of which consi	 Of which consistent 	1 variable		
 User data per job Max. 64 Kbytes Of which consistent 1 variable (462 bytes) Via FCA G SEND and AG_RECV, max. via 10 CP 443-1 or 443-5) User data per job Max. 8 Kbytes Of which consistent 240 bytes Yes (via CP and loadable FB) Interfaces Interface The accumulated number of output bytes are of the interface (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Yes (via CP and loadable FB) Interface Interface The faces Interface The face Max. 150 mA Yes (via CP and loadable FB) Yes (via CP and loadable FB) Interface Interface Interface The face Max. 150 mA Yes VDC) Number of connection MPI: 44 Yes a diagnostic repeater in the strand reduces the number of connection resources by 1 Functionality MPI Yes PROFIBUS DP DP Master/DP slave Interface MPI Mode Interface MPI Mode Interface MPI Mode Interface MAX. 32 bytes Of which consistent 32 bytes 	S7 communication	Yes		
 Of which consistent 1 variable (462 bytes) S5-compatible via FC AG_SEND and CP 443-1 or 443-5) User data per job Max. 8 Kbytes Of which consistent 240 bytes Standard communication Yes (via CP and loadable FB) Interfaces Interfaces Interface Interface Interface Interface The maximum address area of the interface (max. 2KB inputs/2 KB outputs) accumulated by 32 slaves may not be exceed 244 The accumulated number of output bytes area of the interface (Max. 8 Kbytes Interfaces Interfaces Interface The maximum address area of the interface (Max. 2KB inputs/2 KB outputs) accumulated by 32 slaves may not be exceeded Vau can only configure the CPU once as a DP slave Vou can only configure the CPU once as a DP slave if the CPU has several interfaces. Utilities PROFIBUS DP MPI Yes PROFIBUS DP DP master/DP slave Interface MPI Mode Viser data per address area Of which consistent 32 bytes Address area Of which consistent 32 bytes address area Of which consistent 32 bytes Interface Type of interface Type of interface Programming device/OP communication Routing Yes via SFC X_SEND, communication ST basic Yes via SFC X_SEND, Yes via SFC X_SEND, Yes via SFC X_SEND, Yes via SFC X_SEND,	 User data per job 	Max. 64 Kbytes		
S5-compatible communication via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5) • The accumulated number of output bytes at the slots may not exceed 244 • Of which consistent 240 bytes - Of which consistent 240 bytes Standard communication (FMS) Yes (via CP and loadable FB) Interfaces Yes (via CP and loadable FB) Interface Interface Type of interface Interface Type of interface Integrated Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA IS VDC to 30 VDC) Max. 150 mA Number of connection repeater in the strand reduces the number of connection resources by 1 • Utilities - Programming device/OP communication Yes • MPI Yes ves • Programming device/OP communication Yes - St basic communication - Routing - St basic communication Yes via SFC X_SEND, communication - St basic communication Yes via SFC X_SEND, communication Yes via SFC X_SEND, communication - St basic communication Yes via SFC X_SEND, communication Yes via SFC X_SEND, communication - St basic communication Yes via SFC	 Of which consistent 	1 variable (462 bytes)		
 Oser data per jub max. Shoyles Of which consistent 240 bytes Standard communication Yes (via CP and loadable (FB) Interfaces Interface Intermediate memory Intermediate memory Intermediate memory Interface /ul>	S5-compatible	via FC AG_SEND and AG_RECV, max. via 10	number of output bytes at the slots may not	
- Of Whiter Consistent 240 bytes Standard communication Yes (via CP and loadable FB) Interfaces outputs) accumulated by 32 slaves may not be exceeded Interface Integrated Type of interface Integrated Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) MPI: 44 resources DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1 - Functionality ODB (GSD) file http://www.ad.sieme si_e/gsd PROFIBUS DP DP master/DP slave Ithinterface MPI Mode - Utilities - Programming device/OP communication Yes - - Routing device/OP communication Yes - - Routing device/OP communication Yes via SFC X_ SEND, communication - S7 basic communication Yes via SFC X_ SEND, communication Yes via SFC X_ SEND, communication - S7 basic Yes via SFC X_ SEND, communication Yes via SFC X_ SEND, communication Max. 150 mA	 User data per job 	Max. 8 Kbytes		
Standard communication Yes (via CP and loadable FB) (max. 2KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded Interfaces 1st Interface Stanterface Type of interface Integrated by 32 slaves may not be exceeded Type of interface Integrated Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) 0 Number of connection MPI: 44 reduces the number of connection resources by 1 Functionality ODB (GSD) file http://www.ad.sieme si_e/gsd MPI Yes PROFIBUS DP DP master/DP slave Utilities - - Programming device/OP communication Yes - - Routing device/OP communication Yes - - Routing they for interface Max. 32 - Of which consistent sloolated 32 bytes - Type of interface Integrated Physical RS 485/Profibus Isolated Yes - State device/OP communication Yes via SFC X_SEND, communication Yes via SFC X_SEND	 Of which consistent 	240 bytes		
Interfaces1st InterfaceType of interfacePhysicalRS 485/ProfibusIsolatedYesPower supply to interfaceMax. 150 mA(15 VDC to 30 VDC)MPI: 44Number of connectionMPI: 44resourcesDP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1FunctionalityODB (GSD) fileMPIYesPROFIBUS DPDP master/DP slave1st Interface MPI ModeVirtual slotsMPIYesPROFIBUS DPDP master/DP slaveItst Interface MPI ModeVirtual slotsMax. 32-UtilitiesProgramming redivice/OP communication-RoutingYesS7 basic communication-S7 basic communication-			(max. 2KB inputs /2 KB	
Type of interface Integrated Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) MPI: 44 resources DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1 MPI Functionality ODB (GSD) file http://www.ad.sieme si_e/gsd • MPI Yes • PROFIBUS DP DP master/DP slave • Utilities - Virtual slots Max. 32 • Utilities - Virtual slots Max. 32 • Utilities - Of which consistent 32 bytes • Of which consistent 32 bytes • Global data Yes - Of which consistent 32 bytes • S7 basic Yes via SFC X_SEND, communication Yes via SFC X_SEND, communication Max. 150 mA • S7 basic Yes via SFC X_SEND, communication Max. 150 mA Yes	Inter	faces	by 32 slaves may not	
Physical RS 485/Profibus Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) MPI: 44 resources DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1 – Monitor/modify Yes • Utilities – Routing Yes • PROFIBUS DP DP master/DP slave • Utrual slots Max. 32 • Utilities – Virtual slots Max. 32 – User data per address area – Of which consistent 32 bytes • Utilities – Of which consistent 32 bytes – • Routing Yes – Of which consistent 32 bytes • Global data Yes – Type of interface Integrated • S7 basic Yes via SFC X_SEND, communication Yes via SFC X_SEND, communication Yes via SFC X_SEND, x_RCV, X_GET and Max. 150 mA	1st Int	erface		
In the log relationIsolatedYesPower supply to interfaceMax. 150 mA(15 VDC to 30 VDC)MPI: 44Number of connectionMPI: 44resourcesDP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1FunctionalityYesPROFIBUS DPDP master/DP slaveIst Interface MPI Mode-Utilities-Programming device/OP communicationYes-Programming device/OP communication-Routing yes-S7 basic communication-S7 basic communicat	Type of interface	Integrated		
Isolated Yes Power supply to interface Max. 150 mA Power supply to interface Max. 150 mA (15 VDC to 30 VDC) MPI: 44 Number of connection MPI: 44 repeater in the strand reduces the number of connection resources by 1 Power supply to interface Functionality ODB (GSD) file MPI Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode - Virtual slots Utilities - User data per address area - Programming device/OP communication Yes - Routing Yes - Routing Yes - S7 basic Yes via SFC X_SEND, communication S2 END, X_RCV, X_GET and	Physical	RS 485/Profibus	, ,	
 Prover supply to interface indix. ISO INA (15 VDC to 30 VDC) Number of connection MPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1 Functionality MPI Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode Utilities Programming Yes Utilities Vitilities Programming Yes Of which consistent 32 bytes Integrated Physical RS 485/Profibus Isolated Yes Solated Yes Power supply to interface MAX. 150 mA 	Isolated	Yes		aces.
Number of connection resourcesMPI: 44 DP: 32 a diagnostic repeater in the strand reduces the number of connection resources by 1- Programming RoutingYesFunctionality- DDB (GSD) filehttp://www.ad.siemer si_e/gsdMPIYesPROFIBUS DPDP master/DP slave1st Interface MPI Mode- Virtual slotsMax. 32- Programming device/OP communicationYes- RoutingYes- RoutingYes- RoutingYes- S7 basic communicationYes via SFC X_SEND, communication- S7 basic communicationYes via SFC X_SEND, x_RCV, X_GET and		Max. 150 mA		
 Additional of connection in the trand reduces the number of connection resources by 1 Functionality MPI Yes PROFIBUS DP DP master/DP slave Ist Interface MPI Mode Utilities Programming device/OP communication Routing Yes Of which consistent 32 bytes Of which consistent 32 bytes Of which consistent 32 bytes Type of interface MSA 485/Profibus Isolated Yes Solated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) 			-	
repeater in the strand reduces the number of connection resources by 1FunctionalityDDB (GSD) filehttp://www.ad.sieme si_e/gsdFunctionalityODB (GSD) filehttp://www.ad.sieme si_e/gsdMPIYesUp to 12 MbpsPROFIBUS DPDP master/DP slaveIntermediate memory244 bytes inputs/244 outputsUtilities-Virtual slotsMax. 32Programming device/OP communicationYes-Of which consistent32 bytes-Routing communicationYes-Of which consistent32 bytes-S7 basic communicationYes via SFC X_SEND, communicationIntegratedPower supply to interface Max. 150 mAMax. 150 mA			0 0	
reduces the number of connection resources by 1 Interview of connection resources by 1 Functionality Transmission rate Up to 12 Mbps • MPI Yes Intermediate memory 244 bytes inputs/244 outputs • PROFIBUS DP DP master/DP slave - Virtual slots Max. 32 • Utilities - Virtual slots Max. 32 bytes • Utilities - Of which consistent 32 bytes • Of which consistent 32 bytes - • Global data Yes - Type of interface Integrated • Physical RS 485/Profibus Isolated Yes • S7 basic Yes via SFC X_SEND, communication X_RCV, X_GET and Max. 150 mA	resources		0	
FunctionalityMPIYesPROFIBUS DPDP master/DP slaveIst Interface MPI Mode-UtilitiesProgramming device/OP communication-RoutingYesGlobal data communication-S7 basic communication-S7 basic communication-Yes via SFC X_SEND, communication-S7 basic communication-S7 basic communication-Yes via SFC X_SEND, communication-Yes via SFC X_GET and		reduces the number of		
 MPI Yes outputs / 244 bytes inputs / 244 bytes /	Functi	,		
1st Interface MPI Mode - Virtual slots Max. 32 • Utilities - User data per address area - User data per address area - - Programming device/OP communication Yes - Of which consistent 32 bytes - Routing Yes - Of which consistent 32 bytes - Global data yes communication Yes - - S7 basic yes via SFC X_SEND, communication Yes via SFC X_GET and Power supply to interface Max. 150 mA (15 VDC to 30 VDC)	• MPI	Yes		•
 Utilities Programming device/OP communication Routing Yes Global data communication S7 basic communication X_RCV, X_GET and Description of the second seco		•		
device/OP communication 2nd Interface - Routing Yes - Global data communication Yes - S7 basic communication Yes via SFC X_SEND, communication - S7 basic communication Yes via SFC X_SEND, X_RCV, X_GET and	Utilities		address area	,
- Routing Yes - Global data Yes - Global data Yes - S7 basic Yes via SFC X_SEND, communication - S7 basic Yes via SFC X_GET and	5 5	Yes		
 Routing Yes Global data Yes S7 basic Communication X RCV, X GET and Type of interface Integrated Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) 				terface
 Global data Yes communication S7 basic Yes via SFC X_SEND, communication X_RCV, X_GET and Physical RS 485/Profibus Isolated Yes Power supply to interface Max. 150 mA (15 VDC to 30 VDC) 		Ves	Type of interface	Integrated
communication Isolated Yes - S7 basic Yes via SFC X_SEND, communication Power supply to interface Max. 150 mA (15 VDC to 30 VDC)	•		Physical	RS 485/Profibus
 S7 basic Yes via SFC X_SEND, communication X_RCV, X_GET and Power supply to interface Max. 150 mA (15 VDC to 30 VDC) 		165	Isolated	Yes
	 S7 basic 	X_RCV, X_GET and		Max. 150 mA
– S7 communication Yes	07	-		

	where of composition	00 a dia mandia nana ataw in		0
res	mber of connection	32, a diagnostic repeater in the strand reduces the	 WR_DPARM DPNBM_DG 	2
100		number of connection	DPNRM_DGRDSYSST	8 1 to 8
		resources by 1		1
		onality		See instruction list
•	PROFIBUS DP	DP master/DP slave	System function blocks (SFB)	See instruction list
		P Master Mode	Number of SFBs active at	
•	Utilities		the same time	
	 Programming 	Yes	RD REC	8
	device/OP communication		WR REC	8
		Vec	User program protection	Password protection
	 Routing S7 basic 	Yes Yes	Access to consistent data	Yes
	- S7 basic communication	fes	in the process image	
	 S7 communication 	Yes	CiR synchro	nization time
	 Constant bus cycle 	Yes	Base load	100 ms
	time		Time per I/O byte	40 µs
	 SYNC/FREEZE 	Yes	Clock syr	nchronism
	 Enable/disable DP slaves 	Yes	User data per clock synchronous slave	Max. 244 bytes
•	Transmission rates	Up to 12 Mbps	Maximum number of bytes	The following applies:
•	Number of DP slaves	Max. 125	and slaves in a process	Number of bytes/50 +
•	Address area	Max. 8 Kbytes inputs/ 8	image partition	number of slaves
		Kbytes outputs	Constant bus cycle time	Yes
•	User data per DP slave	Max. 244 bytes inputs,	Shortest clock pulse	1 ms
•	User data per DP slave	max.244 bytes outputs,		0.5 ms without use of
		max. 244 slots each with max. 128 bytes	see manual Clock Synchronism	SFC 126, 127
No			Dimensions	
•		er of input bytes at the slots	Mounting dimensions	50×290×219
•	may not exceed 244	or of output by too of the clote	W×H×D (mm)	
•	may not exceed 244	er of output bytes at the slots	Slots required	2
•		rea of the interface (max.	Weight	approx. 1,07 kg
	8 KB inputs /8 KB output	s) accumulated by 125	Voltages	, Currents
	slaves may not be excee	eded	Current consumption from	Typ. 1.5 A
	2nd Interface I	DP Slave Mode	S7-400 bus (5 VDC)	Max. 1.7 A
As	for the 1st interface		Current consumption from the S7-400 bus (24 VDC)	Total current consumption of the components
	3rd Int	terface	The CPU does not	connected to the MPI/DP
	be of interface	Plug-in interface submodule	consume any current at	interfaces, with a maximum
	ertable interface	IF-964-DP	24 V, and it only makes this voltage available at the	of 150 mA per interface
	omodule		MPI/DP interface.	
Tec	chnical features as for the		Backup current	Typically 600 μA
_		terface		Maximum 1810 μA
	be of interface	Plug-in interface submodule	Incoming supply of external	5 VDC to 15 VDC
	ertable interface omodule	IF-964-DP	backup voltage to the CPU	
Sur	chnical features as for the	and interface	maximum backup time	See manual Module
Too	annean leannes as ior the			Specifications, chapter 3.3
Tec				
	Progra	imming	Power loss	Typ. 6.0 W
Pro	Progra ogramming language	Imming LAD, FBD, STL, SCL	Power loss	Typ. 6.0 W
Pro	Progra ogramming language truction set	LAD, FBD, STL, SCL See instruction list	Power loss	Тур. 6.0 W
Pro Inst Bra	Progra ogramming language truction set acket levels	LAD, FBD, STL, SCL See instruction list 8	Power loss	Тур. 6.0 W
Pro Inst Bra Sys	Progra ogramming language truction set acket levels stem functions (SFC)	LAD, FBD, STL, SCL See instruction list	Power loss	Тур. 6.0 W
Pro Inst Bra Sys Nut the	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every	LAD, FBD, STL, SCL See instruction list 8	Power loss	Тур. 6.0 W
Pro Inst Bra Sys Nut the stra	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and	LAD, FBD, STL, SCL See instruction list 8 See instruction list	Power loss	Тур. 6.0 W
Pro Inst Bra Sys Nut the stra	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and DPSYC_FR	LAD, FBD, STL, SCL See instruction list 8 See instruction list	Power loss	Тур. 6.0 W
Pro Inst Bra Sys Nui the stra •	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and DPSYC_FR D_ACT_DP	LAD, FBD, STL, SCL See instruction list 8 See instruction list 2 4	Power loss	Тур. 6.0 W
Pro Insi Bra Sys Nui the stra •	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and DPSYC_FR D_ACT_DP RD_REC	LAD, FBD, STL, SCL See instruction list 8 See instruction list 2 4 8	Power loss	Тур. 6.0 W
Pro Inst Bra Sys Nut the stra •	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and DPSYC_FR D_ACT_DP RD_REC WR_REC	LAD, FBD, STL, SCL See instruction list 8 See instruction list 2 4 8 8	Power loss	Typ. 6.0 W
Pro Inst Bra Sys Nut the stra •	Progra ogramming language truction set acket levels stem functions (SFC) mber of SFCs active at same time for every and DPSYC_FR D_ACT_DP RD_REC	LAD, FBD, STL, SCL See instruction list 8 See instruction list 2 4 8	Power loss	Typ. 6.0 W

6.8 Technical Specifications of the Memory Cards

Name	Order Number	Current Consumption at 5 V	Backup Currents
MC 952 / 64 Kbytes / RAM	6ES7952-0AF00-0AA0	Typ. 20 mA Max. 50 mA	Typ. 0.5 μΑ Max. 20 μΑ
MC 952 / 256 Kbytes / RAM	6ES7952-1AH00-0AA0	Typ. 35 mA Max. 80 mA	typ. 1 μΑ Max. 40 μΑ
MC 952 / 1 Mbyte / RAM	6ES7952-1AK00-0AA0	Typ. 40 mA Max. 90 mA	Тур. 3 µA Max. 50 µA
MC 952 / 2 Mbytes / RAM	6ES7952-1AL00-0AA0	Typ. 45 mA Max. 100 mA	Тур. 5 µА Мах. 60 µА
MC 952 / 4 MB / RAM	6ES7952-1AM00-0AA0	Typ. 45 mA Max. 100 mA	Тур. 5 µA Max. 60 µA
MC 952 / 8 MB / RAM	6ES7952-1AP00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 μΑ Max. 60 μΑ
MC 952 / 16 MB / RAM	6ES7952-1AS00-0AA0	Typ. 100 mA Max. 150 mA	Typ. 50 μA Max. 125 μA
MC 952 / 64 MB / RAM	6ES7952-1AY00-0AA0	Typ. 100 mA Max. 150 mA	Typ. 100 μA Max. 500 μA
MC 952 / 64 Kbytes / 5V Flash	6ES7952-0KF00-0AA0	Typ. 15 mA Max. 35 mA	-
MC 952 / 256 Kbytes / 5V Flash	6ES7952-0KH00-0AA0	Typ. 20 mA Max. 45 mA	-
MC 952 / 1 Mbyte / 5V Flash	6ES7952-1KK00-0AA0	Typ. 40 mA Max. 90 mA	-
MC 952 / 2 Mbytes / 5V Flash	6ES7952-1KL00-0AA0	Typ. 50 mA Max. 100 mA	-
MC 952 / 4 Mbytes / 5V Flash	6ES7952-1KM00-0AA0	Typ. 40 mA Max. 90 mA	-
MC 952 / 8 Mbytes / 5V Flash	6ES7952-1KP00-0AA0	Typ. 50 mA Max. 100 mA	-
MC 952 / 16 Mbytes / 5V Flash	6ES7952-1KS00-0AA0	Typ. 55 mA Max. 110 mA	-
MC 952 / 32 Mbytes / 5V Flash	6ES7952-1KT00-0AA0	Typ. 55 mA Max. 110 mA	-
MC 952 / 64 Mbytes / 5V Flash	6ES7952-1KY00-0AA0	Typ. 55 mA Max. 110 mA	-
Dimensions W x H x D W \times H \times D (ir	י ו mm)	7,5 x 57 x 87	
Weight		Max. 35 g	
EMC protection		Provided by con	struction

7

IF 964-DP Interface Submodule

Chapter Overview

Section	You will Find	Page
7.1	IF 964-DP Interface Submodule for S7-400	7-2

7.1 IF 964-DP Interface Submodule for S7-400

Order Numbers

You can use the IF 964-DP interface submodule with order number 6ES7964-2AA04-0AB0 in the S7-400 with firmware V4.0 or higher.

The interface is labeled on the front panel and can therefore be identified in mounted state.

Characteristics

The IF 964-DP interface submodule is used for connecting distributed I/O via "PROFIBUS DP". The submodule has an isolated RS485 interface. The maximum transmission rate is 12 Mbps.

The permissible cable length depends on the transmission rate and the number of nodes. In the case of a point-to-point connection with a speed of 12 Mbps, a cable length of 100 m is possible, and with a speed of 9.6 Kbps a cable length of 1,200 m is possible.

The system can be expanded to 125 stations.

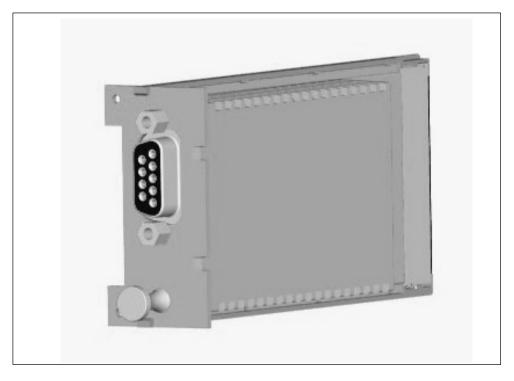


Figure 7-1 IF 964-DP Interface Submodule

Note

Even in an S7-400 CPU you may remove or insert the IF 964-DP interface submodule only if it is **off circuit**.

If you remove the interface submodule while the power supply is switched on, the CPU goes into DEFECTIVE mode.

Additional Information

You can find information on "PROFIBUS DP" in the following technical overviews or manuals:

- DP master manuals, for example, *S7-300 Programmable Controller* or *S7-400, Programmable Controllers* for the PROFIBUS-DP interface
- Manuals on the DP slaves, for example, ET 200M Distributed I/O Device or ET 200C Distributed I/O Device
- STEP 7 manuals

7.1.1 Pin Assignments

X1 Connector

There is a 9-pin sub D socket connector on the frontside of the submodule for plugging in the connecting cable. See Table 7-1 for the pin assignments.

Pin	Signal	Meaning	Direction
1	-		
2	M 24	24 V reference potential	Output
3	LTG_B	Line B	Input/Output
4	RTSAS	Request to send (AS)	Output
5	M5 _{ext}	Operational ground (isolated)	Output
6	P5 _{ext}	+ 5 V (isolated), max. 90 mA (for supplying the bus terminator)	Output
7	P 24 V	+24 V, max. 150 mA, non-isolated	Output
8	LTG_A	Line A	Input
9	-		

Table 7-1 X1 Socket, IF 964-DP (9-Pin Sub D Connector)

7.1.2 Technical Specifications

Technical Specifications

The IF 964-DP interface submodule receives its supply voltage from the CPU. The current consumption given in the technical specifications is the consumption required for dimensioning the power supply.

Dimensions and weights		Voltages, Currents	
Dimensions	26 x 54 x 130	Power supply	provided by the S7-400
W x H x D (mm)		Current sink on S7-400 bus	accumulated current
Weight	0.065 kg	The module does not draw cur- rent at 24 V, it merely supplies	consumption of com- ponents connected to
Performance		this voltage to the DP interface	the DP interface, but
Transmissoin rate	9.6 kbps to 12 Mbps		max. 150 mA
Cable length			
 at 9.6 kbps 	max. 1200 m	Load capability on 5 V (floa- ting) (P5 _{ext}) Load capability on 24 V	max. 90 mA max.150 mA
 at 12 Mbps 	max. 100 m		
Number of stations	\leq 125 (depends on the CPU used)		
Interface physics	RS485	Power loss	1 W
Potential isolation	yes		

Index

Α

Address area, CPU 31x-2, 3-3

В

Block stack, 4-4 BUSF, 3-8, 3-18

С

Calculation, reaction time, 5-12 CiR, 2-7 Cold restart, operating sequence, 1-16 Cold start, 1-16 Communications via MPI and via communication bus, cycle load, 5-4 Configuration frame. See on the Internet at http://www.ad.siemens.de/simatic-cs Consistent data, 3-34 Access to the working memory, 3-35 Communication block, 3-35 Communication function, 3-35 DP standard slave, 3-35 Process image, 3-37 SFC 14 "DPRD_DAT", 3-35 SFC 15 "DPWR DAT", 3-36 SFC 81 "UBLKMOV", 3-34 CPU, mode selector, 1-13 CPU 315-2 DP See auch CPU 31x-2 DP master, 3-4 CPU 316-2 DP. See CPU 31x-2 CPU 318-2. See CPU 31x-2 CPU 31x-2 bus interruption, 3-12, 3-22, 3-32 diagnostic addresses for PROFIBUS, 3-11, 3-21 Direct communication, 3-31 DP address areas, 3-3 DP master diagnosis with STEP 7, 3-9 diagnostics using LEDs, 3-8 DP slave, 3-13 diagnostics using LEDs, 3-18 diagnostics with STEP 7, 3-18 intermediate memory, 3-14

operating mode changes, 3-12, 3-22, 3-32 CPU parameters, 1-23 Cross–communication. *See* Direct communication Cycle load, communications via MPI and communication bus, 5-4 Cycle Time, increasing, 5-4 Cycle time, 5-2 calculation example, 5-18 calculation examples, 5-17 parts, 5-3

D

Data transfer, direct, 3-31 Diagnosis module, CPU 315-2 DP as DP slave, 3-27 station, CPU 31x-2 as slave, 3-28 Diagnostic addresses, CPU 31x-2, 3-11, 3-21 Diagnostic interrupt, CPU 31x-2 as DP slave, 3-29 Diagnostic interrupt reaction time, 5-23 Diagnostics, direct communication, 3-32 **Direct communication** CPU 31x-2, 3-31 diagnostics, 3-32 DP interface, 1-22 **DP** master CPU 31x-2, 3-4 diagnosis with STEP 7, 3-9 diagnostics using LEDs, 3-8 DP slave CPU 31x-2, 3-13 diagnostics using LEDs, 3-18 diagnostics with STEP 7. 3-18 DP slave diagnosis, structure, 3-23 DP standard slave, Consistent data, 3-35

Ε

Error displays, CPU 41x-3 and 41x-4, 1-12 error displays, 1-11

F

Flash card, 1-18

Η

Hardware interrupt processing, 5-22 Hardware interrupt reaction time, 5-21 of CPUs, 5-21 of signal modules, 5-22 of the CPUs, 5-22 Hot restart, 1-16

I

I/O direct accesses, 5-16
IF 964-DP, 7-2 additional information, 7-3 characteristics, 7-2 pin assignments, 7-3 technical specifications, 7-4
Intermediate memory CPU 31x-2, 3-14 for data transfer, 3-14
Interrupts, CPU 315-2 DP as DP slave, 3-30

Μ

Master PROFIBUS address, 3-25 Memory areas, 4-2 Memory card, 1-17 Memory reset, operating sequence, 1-14 Module diagnosis, CPU 31x-2 as DP slave, 3-27 Monitoring functions, 1-8 MPI interface, 1-21 MPI-Parameter, 1-15 Mulitcomputing, 2-3 Multicomputing interrupt, 2-6

0

Operating system, scan time, 5-6 Order number 6ES7 412-1XF03-0AB0, 6-2 6ES7 412-2XG00-0AB0, 6-6 6ES7 414-2XG03-0AB0, 6-10 6ES7 414-3XJ00-0AB0, 6-14 6ES7 416-2XK02-0AB0, 6-18 6ES7 416-3XL00-0AB0, 6-22 6ES7 417-4XL00-0AB0, 6-26 Order numbers CPUs, 6-1 Memory Cards, 6-30

Ρ

Parameter assignment frame. *See* on the Internet at http://www.ad.siemens.de/simatic-cs Parameters, 1-23 Process image updating, processing time, 5-4, 5-5 Process interrupt, CPU 31x-2 as DP slave, 3-29 Processing time process image updating, 5-4, 5-5 user program, 5-4 Protection level, 1-14 setting, 1-14

R

RAM card, 1-18 Reaction time, 5-12 calculation, 5-12 calculation of, 5-14, 5-15 diagnostic interrupt, 5-23 hardware interrupt, 5-21 longest, 5-15 parts, 5-12 reducing, 5-16 shortest, 5-14 Reboot, operating sequence, 1-16 Restart, 1-16 operating sequence, 1-16

S

Scan cycle control, scan time, 5-6 Scan time, operating system, 5-6 Service data, 2-2 SFC 81 "UBLKMOV", 3-34 Station diagnosis, CPU 31x-2 as DP slave, 3-28 station states 1 to 3, 3-24 Status LEDs, all CPUs, 1-10

Т

Technical specifications CPU 412-1, 6-2 CPU 412-2, 6-6 CPU 414-2, 6-10 CPU 414-3, 6-14 CPU 416-2, 6-18 CPU 416-3, 6-22 CPU 417-4, 6-26 CPUs, 6-1 IF 964-DP, 7-4 Memory Cards, 6-30

U

User program processing time, 5-4

Automation System S7-400 CPU Specifications A5E00267840-03